DIGITAL TELEVISION SYSTEMS AND INFOCOMMUNICATION DEVICES

# CW-4901


## Version 2.00

## Instruction Manual

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## Using this Document

This document is intended for the software and hardware engineer’s reference and provides detailed information about the Gigabit Ethernet Controller. Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact ByteStudio (bytestudio@bytestudio.hu) for additional information that may help in the development process.

# 1. Introduction

ByteStudio has developed a special solution for processing the digital television signals, where both the transmission of the high data rate transport stream and the control of the associated devices will be done over Ethernet network. The BS-GEC-4x Gigabit Ethernet Controller is a universal data transmission and device controller module for IP based digital television systems.

In the BS-GEC-4x the communication is handled by the IP Manager. The IP Manager serves the connected four transport stream transmitter/receiver units of identical set-up and extremely high data rate. For the device control over the IP network, the module provides a serial and a parallel port, an $I^2C$ bus, an 8-bit selector port and an output for driving LEDs.

The board cannot accommodate all connectors of the four transmitter/receiver units therefore it is manufactured in two versions (4I and 4O). The 4I version is equipped with 4 inputs, and it can process and pack in UDP/IP packets 4 transport streams coming from different sources. The 4O version is equipped with 4 outputs, and from the input gigabit data stream it can assemble 4 output transport streams upon the IP addresses and Port numbers. The 4-input version is equipped also with a TS output of full value.

Gigabit Ethernet Controller operates in IPv4, but is already prepared to IPv6. Recognition of the systems with 10, 100 and 1000 Mbit/s data rate is automatic (Auto Negotiation), and the controller goes always to the applicable highest data rate full duplex mode. The controller handles the ARP and Ping instructions, and it is equipped with an ARP Advertisement function of programmable repetition time. Both the Primary and the Secondary MAC address of the module are programmable. The module is suitable for receiving and transmitting the transport stream in unicast and multicast systems alike; in multicast networks calling in the transport stream is made with IGMP messages. The four transport stream sending units are equipped with own sync separator, null packet remover and packet clipper. The number of packets to be built in the UDP/IP packets is programmable between 1 and 7.

The controller handles the SNMP messages: each instruction of the instruction set can be built in SNMP messages and the error messages are delivered by sending SNMP Trap.

The instructions start with DDToIP (Digital Data Transmission over IP) characters, after which the user can put a character series for the identification of his system.

## 2. Features

- Single 3.3 V power supply
- Integrated 10Base-T, 100Base-TX and 1000Base-T Ethernet transceiver (supports Auto-Negotiation, Crossover Detection and Auto-Correction)
- 4 programmable NCOs (120 Hz – 62.5 MHz)
- 4 independent Transport Stream (TS) inputs and 1 TS output (GEC-4I)
  TS to UDP/IP converter supports both CW-Net format (with user defined length) and IPTV format (1..7 TS packets, 188/204 bytes mode, null packet remover, transparent transfer).
- 4 independent TS outputs (GEC-4O)
  UDP/IP to TS converter supports unicast, broadcast and multicast reception using IGMPv2 protocol. Programmable output formats (null packet filtering and insertion, gated clock, data valid pin etc.).
- Easy to program via UDP/IP or SNMP
- Extended instruction set (Digital Data Transmission over IP - DDToIP)
- User defined string (e.g. company name) is placed in every message
- CW-Net compatible
- Protocols: ICMP ping, ARP, IGMPv2, SNMP, UDP
- IPv6 preparation
- Programmable ARP and IGMP Membership Report advertisement
- Status and overflow LED ports
- UDP or SNMP Trap messages on overflow event
- 8-bit Parallel Data Interface up to 220 kB/s data rate
- Serial Data Interface
- IIC interface (up to 1 MHz serial clock)
- General Purpose Output Port (8 bits)
- Selector Port (9 bits)

# 3. Model List and Block Diagram

Gigabit Ethernet Controller Model List:

| Model | Features |
|---|---|
| 4I | 4 Transport Stream Input Channels<br>1 Transport Stream Output Channel |
| 4O | 4 Transport Stream Output Channels |
| 2D | 2 Transport Stream Input Channels<br>2 Transport Stream Output Channels<br>(Future release) |
| 2L | 2 Transport Stream Output Channels with internal loopback<br>(Future release) |

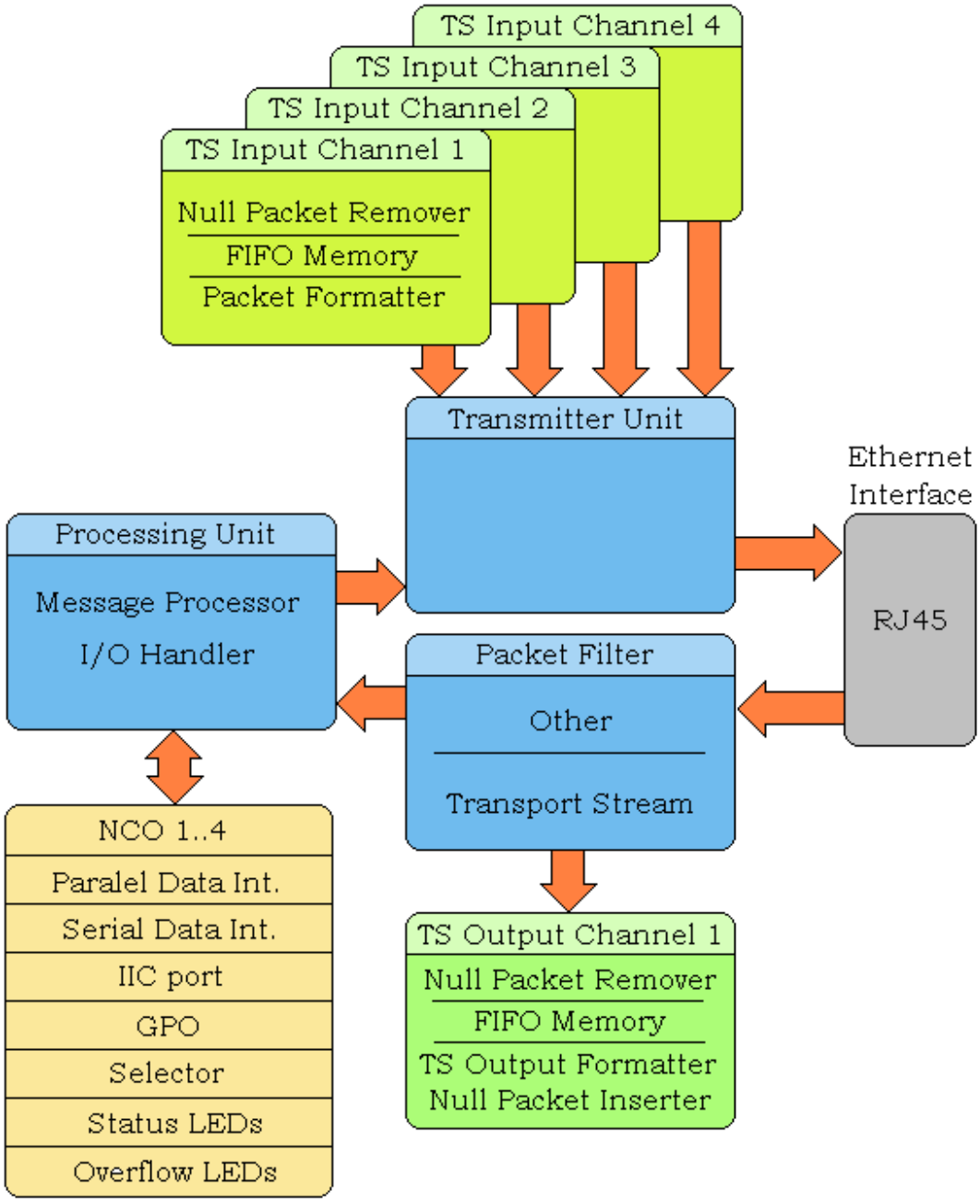



Figure 1. GEC-4I Block Diagram

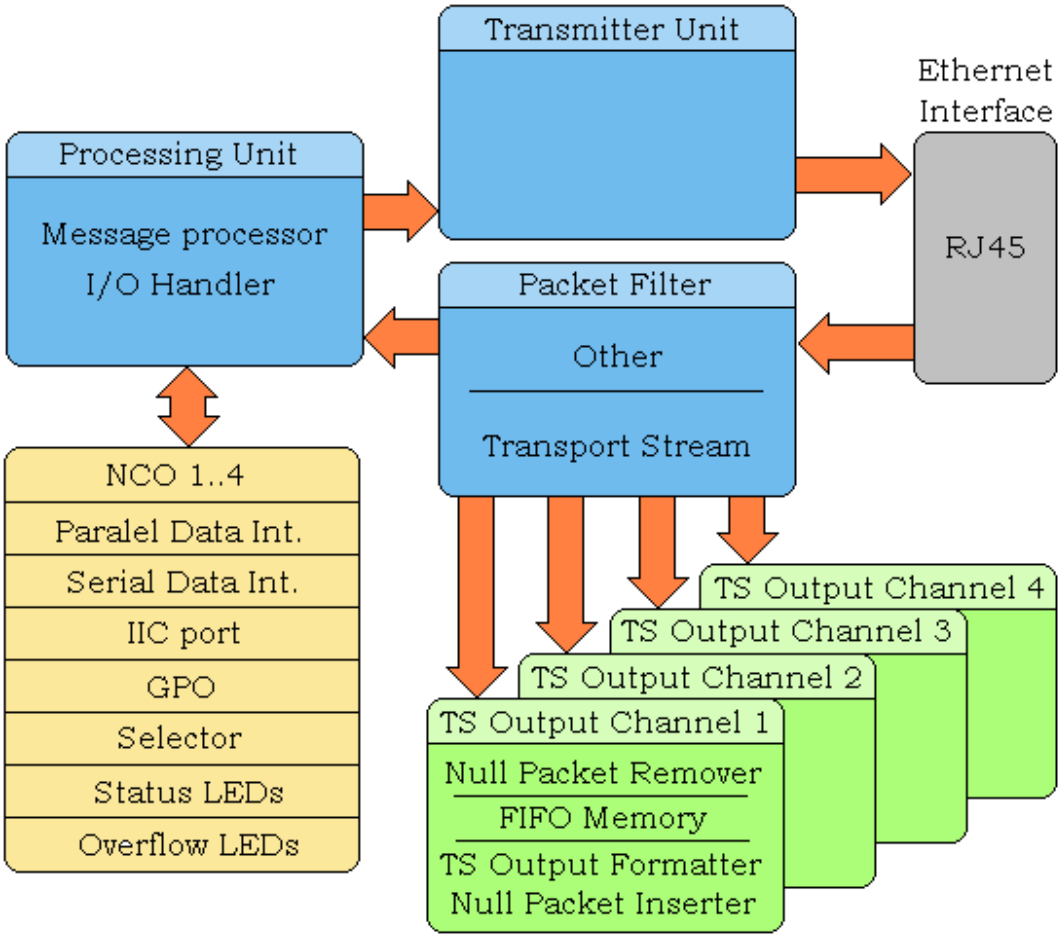



Figure 2. GEC-4O Block Diagram

# 4. General Description

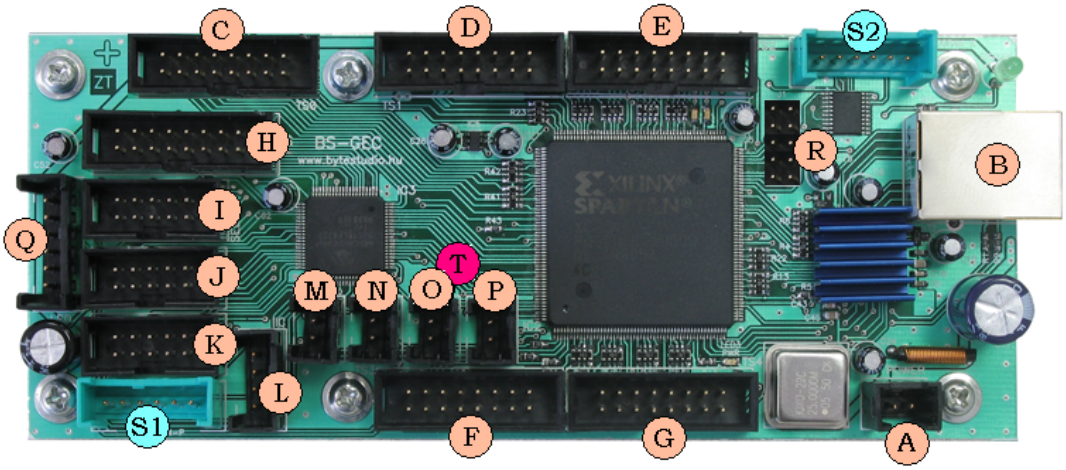



Figure 3. Connectors

| Char | Connector |
|---|---|
| A | POWER |
| B | RJ45 ETHERNET INTERFACE |
| C | TS0 |
| D | TS1 |
| E | TS2 |
| F | TS3 |
| G | TS4 |
| H | PDI (Parallel Data Interface) |
| I | SELECTOR |
| J | SDI (Serial Data Interface) |
| K | GPO (General Purpose Output) |
| L | IIC |
| M | NCO1 |
| N | NCO2 |
| O | NCO3 |
| P | NCO4 |
| Q | STATUSLED |
| R | OVERFLOWLED |
| S1 | *Programming connector (Don't connect!)* |
| S2 | *Programming connector (Don't connect!)* |
| T | Reset Defaults Jumper |
| U | EXTERNAL TRAP (future release) |

## 4.1. Power Supply

The Gigabit Ethernet Controller needs single 3.3 V power supply. Connector (Connector A) pinout:

| Pin | Description | Direction |
|---|---|---|
| 1 | GND | |
| 2 | Power 3.3 V | Input |


Maximum current consumption: 600 mA.

## 4.2. Integrated 10/100/1000 Ethernet Interface

The Gigabit Ethernet Controller contains a Realtek RTL8211B integrated Ethernet transceiver that complies with 10Base-T, 100Base-TX and 1000Base-T IEEE 802.3 standards. Realtek RTL8211B provides all the necessary physical layer functions to over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. The Ethernet interface configuration is the following:

- The Gigabit Ethernet Controller operates in full-duplex mode. Although half-duplex mode is also advertised, working in full-duplex mode is supported only.
- Auto-Negotiation is enabled (advertise all capabilities, prefer Slave). Auto-Negotiation is a mechanism to determine the fastest connection between two devices. The Gigabit Ethernet Controller can transmit and receive Ethernet packets at 10/100/1000Mbps link speed and Auto-Negotiation ensures that the highest priority protocol will be selected.
- Crossover Detection & Auto-Correction are enabled. Ethernet needs a crossover mechanism between both partners to cross the signal transmitted to the receiver when the medium is twisted-pair cable (e.g. CAT.5 UTP). Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices.
- The Gigabit Ethernet Controller automatically corrects polarity errors on the receive pairs in 1000Base-T and 10Base-T modes. In 100Base-TX polarity is irrelevant.

## 4.3. Device Management

Building the network and connecting the devices is made using the standard elements used in computer networks, no special elements or cables are required. For connecting a device UTP (Unshielded Twisted Pair) cables of at least category 5 have to be used. The connections are made with RJ45 8-pin telephony connectors (Connector B). The Gigabit Ethernet Controller supports only the „Full Duplex" mode.

The Gigabit Ethernet Controller can easily be programmed via UDP/IP. Packets can contain one or more instructions. The device supports two instruction protocols:

- CW-Net (see 4.3.2.)
- Digital Data Transmission over IP (see 4.3.3.)

Gigabit Ethernet Controller supports several protocols that do not belong closely to the device management:

- It sends an answer to the ARP query (see RFC 826.).
- It sends an answer to the ICMP PING request (see RFC 792).
- It supports IGMPv2 messages (see RFC 2236).

### 4.3.1. IP and MAC Addresses

The Gigabit Ethernet Controller has two programmable MAC addresses and a programmable IP address.

Primary and secondary MAC addresses can be set using SETPMAC and SETSMAC instructions. The device supports two modes of setting primary MAC address:

- In Manual mode user can freely set the primary MAC address.
- In Auto mode the device automatically computes the primary MAC address from its IP address (figure 4). The firs two bytes of the MAC address are constant 42:57 hexadecimal. The lower 4 bytes refer to the IPv4 address.

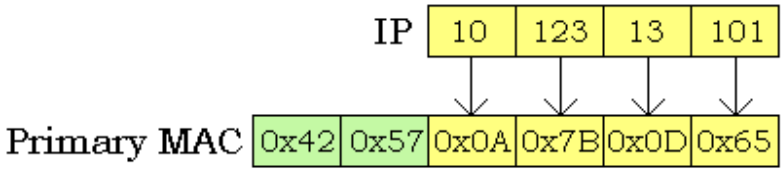



Figure 4. Auto MAC Mode

The secondary MAC address can be configured only manually. However the device receives packets addressed to its secondary MAC, in transmitted packets (e.g. ACK answer, ARP reply, SNMP Trap, TS packet) always the primary MAC address will be included. To disable the secondary MAC address set it to FF:FF:FF:FF:FF:FF.

The IP address can be configured with the SETIP instruction. In the instructions IP addresses are 16-byte long fields because of the IPv6 preparation. In IPv4 systems only the lower four bytes are used as an IPv4 address. The upper 12 bytes must be set to zero. Note that the Internet Assigned Numbers Authority (IANA) has reserved the following three blocks of the IP address space for private networks (see RFC 1918):

| Network Address Range | CIDR Notation |
|---|---|
| 10.0.0.0 - 10.255.255.255 | /8 |
| 172.16.0.0 - 172.31.255.255 | /12 |
| 192.168.0.0 - 192.168.255.255 | /16 |

Factory default settings (MAC addresses are given in hexadecimal format, IP address in decimal format):

- Primary MAC address: 42:57:0A:7B:0D:65
- Secondary MAC address: FF:FF:FF:FF:FF:FF
- IP address: 10.123.13.101

When a packet is received the Packet Filter module (see the block diagram on figure 1.) examines its destination MAC address, size, type and destination UDP port (figure 5.):

- Passed MAC addresses (others are filtered):
  1. Broadcast MAC (FF:FF:FF:FF:FF:FF)
  2. Primary MAC
  3. Secondary MAC
  4. Multicast MAC addresses, if the device is receiving multicast Transport Stream (see RECEIVETS instruction). In this case 01:00:5E:00:00:01 MAC address (“all systems in the subnet”) is also passed.
- Packets with sizes lower than 60 bytes (without CRC) are filtered.
- ICMP Destination Unreachable packets are filtered.
- If a UDP packet is received and its destination port matches with one of the four TS output channel port the packet will be handled as a TS packet. TS output channel ports can be programmed or disabled using RECEIVETS and DONTRECEIVETS instructions. Otherwise if the destination port is not within the TS Port interval the packet will be processed by the Message Processor. Packets

with destination port included in the TS Port interval are dedicated to be foreign TS packets and will be filtered. The TS Port interval can be programmed with the SETTSPORTINTERVAL instruction.

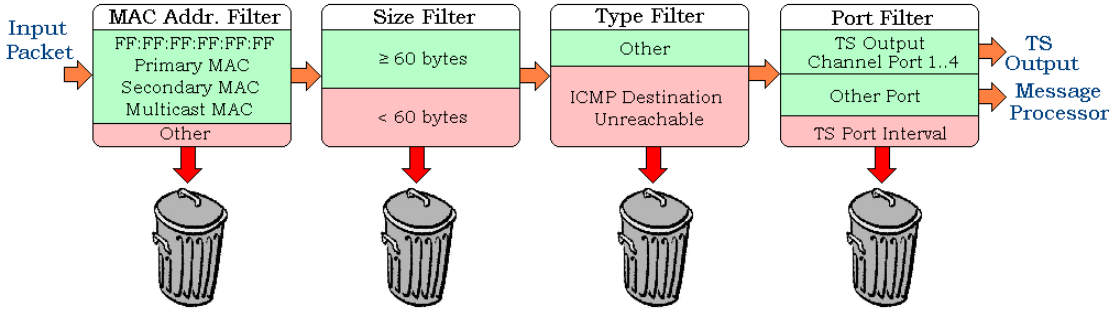



Figure 5. Packet Filter

The Gigabit Ethernet Controller has an ARP Advertising function. If the ARP Advertising function is on, the device periodically sends broadcast ARP reply messages ("the device is at its IP address"). It's useful to refresh switches' MAC address tables.

### 4.3.2. CW-Net Protocol

The CW-Net protocol was developed by CableWorld Ltd.. It performs both device control, data loading and continuous transmission of the transport stream using Ethernet networks and UDP/IPv4 protocol. The Gigabit Ethernet Controller is fully compatible with the CW-Net system with the following restrictions:

- IPTV Option is always included.
- Only TS Channel 1 and NCO1 can be programmed via CW-Net.
- Only the lower 16 bits of the serial number can be set.
- *Replace MAC* instruction changes the Primary MAC Address.
- When using the *Set Outputs* instruction, Out1 port refers to Selector and Out2 port refers to GPO. No clock signals are implemented.

For details about CW-Net visit www.cableworld.eu .

### 4.3.3. DDToIP Protocol

Digital Data Transmission over IP (DDToIP) is a flexible device management protocol specially developed for the Gigabit Ethernet

Controller. The instructions are encapsulated in UDP/IP packets as shown in figure 6.

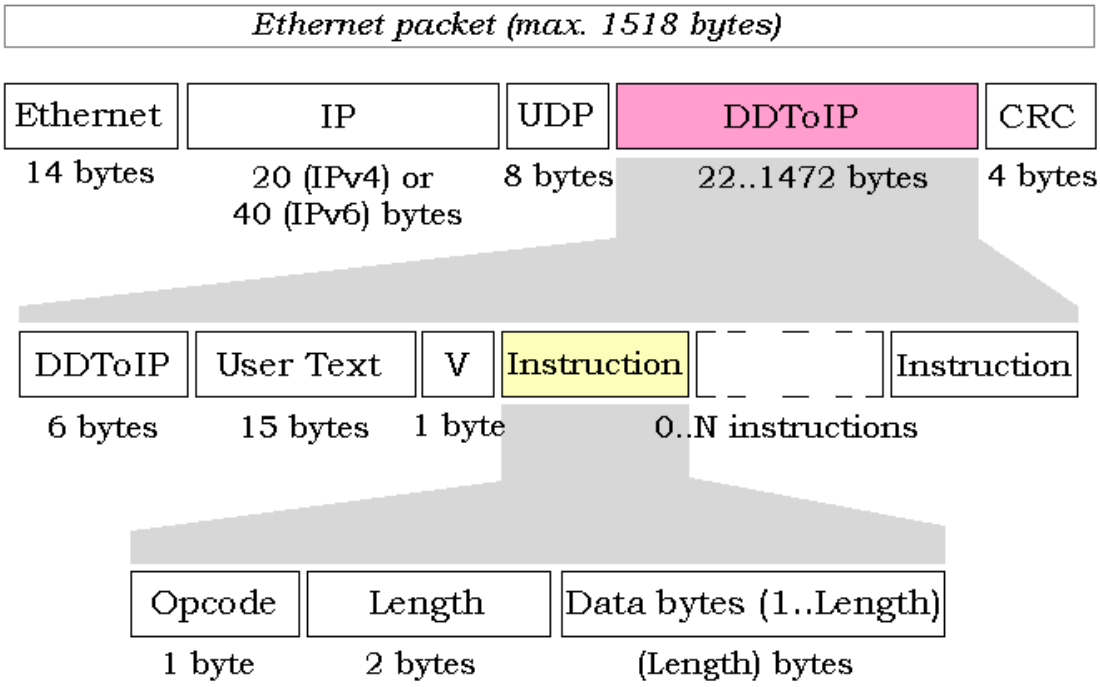



Figure 6. DDToIP Protocol

Data packets start with a standard 14-byte MAC frame (Ethernet header). The MAC frame structure is described in the IEEE 802.3 international standard. The first 6 bytes of the 14-byte Ethernet header carry the address of the device to receive, the next 6 bytes carry the address of the sender device. The last 2 bytes contain a length field or an Ethernet type.

The Ethernet header is followed by an IPv4 or IPv6 header depending on the Ethernet type (0x0800 for IPv4 and 0x86DD for IPv6). The length of the IPv4 header is generally 20 bytes; the IPv6 header's is 40 bytes. IP header carries the destination's IP address and the sender's IP address. Details are described in RFC 768 and RFC 2460.

The UDP header consists of 8 bytes. The structure of the UDP header is described in RFC 768. It contains the source and destination port numbers.

The Ethernet packets are closed with a 4-byte CRC.

The UDP payload must start with "DDToIP" characters (44-44-54-6F-49-50 hexadecimal). It is followed by a 15-character user-defined

string (User Text). You can use this field to place your company name into the UDP packet. V (version number) must be 0x01.

The DDToIP packet can contain one or more instructions. Instructions are performed sequentially. Details are described in section 5.

### 4.3.4. Network Mask and Default Gateway

The network address space is usually organized into several subnets. Routers (default gateways) constitute borders between subnets. In IPv4, the subnet is identified by its base address and network mask. The network mask and default gateway are used only when a SENDTS instruction is processed (to determine the Transport Stream's destination).

While network masks are represented in dot-decimal form their use becomes clearer in binary. Looking at a network address and a network mask in binary the device can determine which part of the address is the network address and which part is the host address. To do this, it performs a bitwise "AND" operation. Network masks consist of a series of 1s in binary followed by 0s. The 1s designate that part of the address as being part of the network portion and the 0s designate that part as being part of the host address. If the Transport Stream's destination address belongs to some place outside the local subnet, the Gigabit Ethernet Controller sends packets to the destination through the default gateway. The network mask can be programmed using the SETNETMASK instruction. The factory default value is 255.0.0.0.

A default gateway is a node (a router) on a network that serves as an access point to another network. A default gateway is used by the device when a Transport Stream packet's destination address is outside the local subnet. Let's see an example:

Device IP: 10.123.13.101
Network mask: 255.0.0.0
Default gateway: 10.123.13.1
Destination A: 10.14.5.6
Destination B: 192.168.1.6

The local IP address range is 10.0.0.0 to 10.255.255.255. The device will send packets addressed to IPs within this range directly (Destination A), by resolving the destination IP address into a MAC address through an ARP sequence. Packets addressed outside of this range, in the example a packet addressed to 192.168.1.6, are sent to the default gateway address, in this case to 10.123.13.1, which is resolved into a MAC

address as usual. Note that the destination IP address will remain 192.168.1.6, it is just the next-hop physical address that is used, in this case it will be the router's interface physical address.

The Default gateway can be programmed using the SETGATEWAY instruction. The device supports two gateway modes:

- Off: There is no default gateway in the network. Packets will be sent directly to destination (factory default setting).
- Manual: User sets the gateway IP's. The gateway MAC address will be found by the device using ARP sequence.

References:

- RFC 950 Internet Standard Subnetting Procedure
- RFC 1812 New Internet Subnetting Procedure
- RFC 950 Utility of Subnets of Internet Networks
- RFC 1101 DNS Encodings of Network Names and Other Types

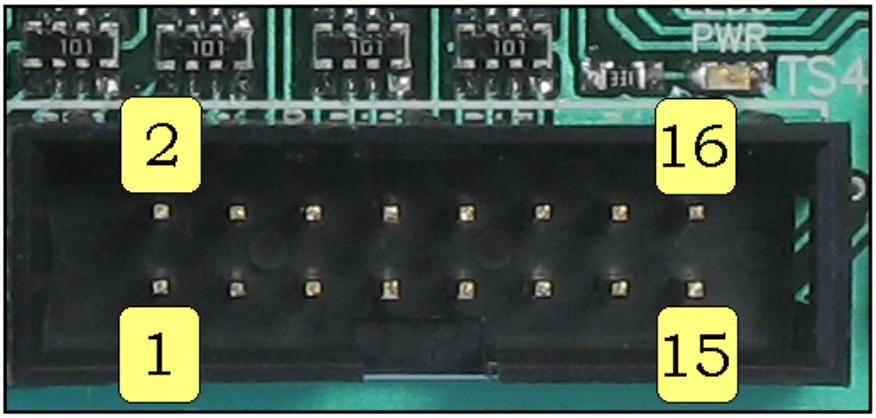
## 4.3. Transport Stream Inputs

The Gigabit Ethernet Controller model 4I (GEC-4I) has four independent Transport Stream (TS) input channels and one Transport Stream output channel. Model 4O (GEC-4O) hasn't got any inputs.

The GEC-4I TS input channels are the TS1, TS2, TS3 and TS4 connectors.

| Connector | Function (GEC-4I) | Direction |
|---|---|---|
| C (TS0) | Transport Stream Output Channel 1 | Output |
| D (TS1) | Transport Stream Input Channel 1 | Input |
| E (TS2) | Transport Stream Input Channel 2 | Input |
| F (TS3) | Transport Stream Input Channel 3 | Input |
| G (TS4) | Transport Stream Input Channel 4 | Input |

Each TS Input channel has a 16-pin AMP type connector. The pinout is the following:




| Pin | Description | Direction | Impedance |
|---|---|---|---|
| 1 | NC (Reserved) | - | - |
| 2 | TS Data 0 | Input | 0 Ω |
| 3 | TS Data 1 | Input | 0 Ω |
| 4 | TS Data 2 | Input | 0 Ω |
| 5 | TS Data 3 | Input | 0 Ω |
| 6 | GND | - | - |
| 7 | Reset | Output | 0 Ω |
| 8 | TS Data 4 | Input | 0 Ω |
| 9 | TS Data 5 | Input | 0 Ω |

| | | | |
|---|---|---|---|
| 10 | TS Data 6 | Input | 0 Ω |
| 11 | TS Data 7 | Input | 0 Ω |
| 12 | TS Data Valid | Input | 0 Ω |
| 13 | TS Clock | Input | 0 Ω |
| 14 | GND | - | - |
| 15 | VDD (3.3 V) | Output | 0 Ω |
| 16 | GND | - | - |

Each Transport Stream input channel has an 8-bit data bus (TS Data 0-7) and control signals: TS Clock, TS Data Valid and Reset.

- TS Clock runs at the rate at which bytes are offered to the device on TS Data 0-7. Data will be sampled (so it must be stable) on the rising edge of the clock signal. TS Clock frequency must be between 0 and 27MHz.
- If Data Valid pin is enabled (see SENDTS instruction), TS Data Valid indicates valid data bytes on TS Data 0-7. TS Data Valid must be at logic 1 for the whole duration of the transport packet. It could go to logic 0 for one or more byte times to indicate data bytes, which should be ignored.
- Reset (active low) is logic 0 during system reset (see RESET instruction).

The Transport Stream input channel converts the input stream to UDP/IP packets (figure 7.). The process depends on the configuration bits (blue text in figure 7.) in the SENDTS instruction.

- If the Data Valid pin is enabled (*DV* = 1) data bytes are ignored while TS Data Valid pin is at logic 0. Otherwise every data byte will be processed.
- *FRMT* bit determines how to encapsulate the TS stream to UDP/IP packets. The Gigabit Ethernet Controller supports IPTV format and CW-Net format.
- In case of CW-Net format the UDP header is followed by n TS data bytes depending on the value of *CWNetSize*. *CWNetSize* must be between 128 and 1440. The UDP payload is closed by a 32 byte *CW frame,* which contains the time stamp of the 125 MHz system clock (*PCR*), the continuity counter and the 'CW-Net' text (figure 8.). *PCR* is encoding timing information as 32 bits of the 125 MHz system clock frequency divided by 5 plus 3 bits for the remainder. *PCR Low* is an 8 bit field and counts from 0 to 4. *PCR High* is a 32 bit field.

PCR(i) = PCR High(i) * 5 + PCR Low (i)

*PCR* indicates the intended time of the arrival of the first data byte in the packet at the TS input channel.
*Note: Because of technical reasons CWNetSize shall not be N*188-32 or N*204-32 (where N is an integer between 1 and 7) if you would like to receive the IP stream with another Gigabit Ethernet Controller! These sizes are reserved for IPTV format packets.*

- In case of IPTV format (after sync separation) null packets and packets with Transport Error Indicator flag set to '1' are being removed if the *RNP* and *RTSP* bits are set. The format converter set the TS packets to 188 (*TSF* = 0) or 204 (*TSF* = 1) bytes in length. The number of TS packets to be built in the UDP/IP packets is programmable between 1 and 7 (*NUMOFPACKET*).

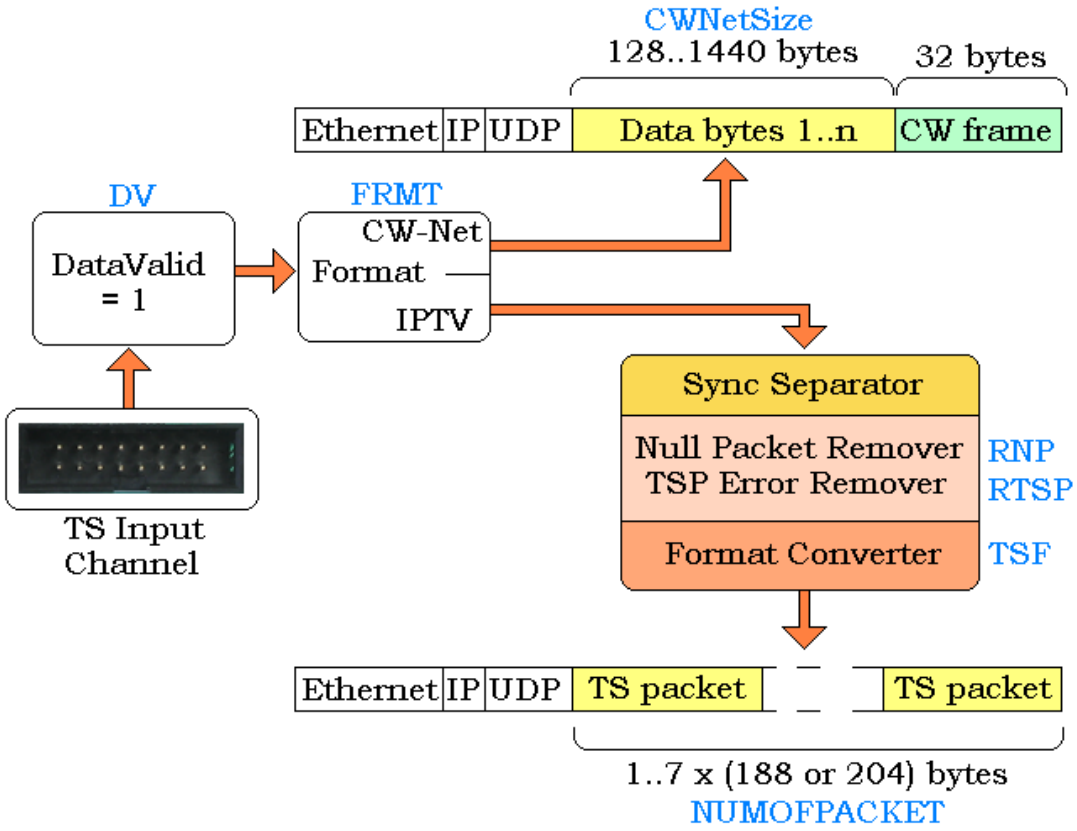



Figure 7. TS input to UDP/IP process

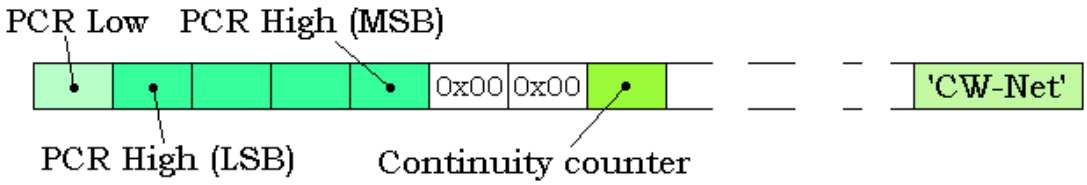



Figure 8. CW frame

The controller starts sending UDP encapsulated TS packets when a SENDTS instruction is received and it stops sending TS when a DONTSENDTS instruction is received or power is off. If the ALWY bit in the SENDTS instruction was set ('1') the controller automatically starts sending TS after a power on state.

The UDP/IP packets can be addressed to the following destinations (*DESTMODE*):

- Send TS to Me: Controller sends TS packets to the host computer. Only the destination UDP port should be set in SENDTS instruction.
- Send to Broadcast: Controller sends TS packets to a broadcast address, which is computed from the device's IP address and the network mask (e.g. IP: 10.123.13.101, Network mask: 255.0.0.0, Broadcast address: 10.255.255.255). The destination MAC address will be FF:FF:FF:FF:FF:FF.
- Send TS to IP: Controller sends TS packets to the selected IP address. The controller sends TS packets addressed to IPs within the local network range directly, by resolving the destination IP address into a MAC address through an ARP sequence. Packets addressed outside of this range are sent to the default gateway address, which is resolved into a MAC address as usual. Destination UDP port and IP address should be set in SENDTS instruction.
- Send TS to Multicast: Controller sends TS packets to the selected multicast IP address. Multicast MAC address is automatically computed from the IP address. Destination UDP port and IP address should be set in SENDTS instruction.
- Send TS to Manual: Controller sends TS packets to the selected manual address. All destination UDP port, IP address and MAC address should be set in SENDTS instruction.

## 4.4. Transport Stream Outputs

The Gigabit Ethernet Controller model 4O (GEC-4O) has four independent Transport Stream output channels; model 4I (GEC-4I) has one Transport Stream output channel.

GEC-4O TS output channels are TS0, TS1, TS2, TS3 and TS4 connectors. TS0 and TS1 are the same outputs. GEC-4I TS output channel is the TS0 connector.

| Connector | Function (GEC-4O) | Direction |
|---|---|---|
| C (TS0) | Transport Stream Output Channel 1 | Output |
| D (TS1) | Transport Stream Output Channel 1 | Output |
| E (TS2) | Transport Stream Output Channel 2 | Output |
| F (TS3) | Transport Stream Output Channel 3 | Output |
| G (TS4) | Transport Stream Output Channel 4 | Output |

| Pin | Description | Direction | Impedance |
|---|---|---|---|
| 1 | NC (Reserved) | - | - |
| 2 | TS Data 0 | Output | 100 Ω |
| 3 | TS Data 1 | Output | 100 Ω |
| 4 | TS Data 2 | Output | 100 Ω |
| 5 | TS Data 3 | Output | 100 Ω |
| 6 | GND | - | - |
| 7 | Reset | Output | 0 Ω |
| 8 | TS Data 4 | Output | 100 Ω |
| 9 | TS Data 5 | Output | 100 Ω |
| 10 | TS Data 6 | Output | 100 Ω |
| 11 | TS Data 7 | Output | 100 Ω |
| 12 | TS Data Valid | Output | 100 Ω |
| 13 | TS Clock | Output | 100 Ω |
| 14 | GND | - | - |
| 15 | VDD (3.3 V) | Output | 0 Ω |
| 16 | GND | - | - |

The Transport Stream output channel has an 8-bit data bus (TS Data 0-7) and control signals: TS Clock, TS Data Valid and Reset. TS Clock frequency refers to NCO frequency. Data changes on the falling edge of the clock signal.

If Data Valid pin is enabled (see RECEIVETS instruction), TS Data Valid indicates valid data bytes on TS Data 0-7. TS Data Valid is at logic

1 for the whole duration of the transport packet and goes to logic 0 during ignored data bytes.

Reset (active low) is logic 0 during system reset (see RESET instruction).

The controller starts receiving TS (Output Channel becomes active, port filter is enabled) after a RECEIVETS instruction is received. For receiving multicast TS the user must set the multicast IP address of the stream and the UDP port number. For receiving normal TS the user must set the UDP port only. The TS Output Channel will be disabled when a DONTRECEIVETS instruction is received ('disabled' means that all output pins are forced to be low).

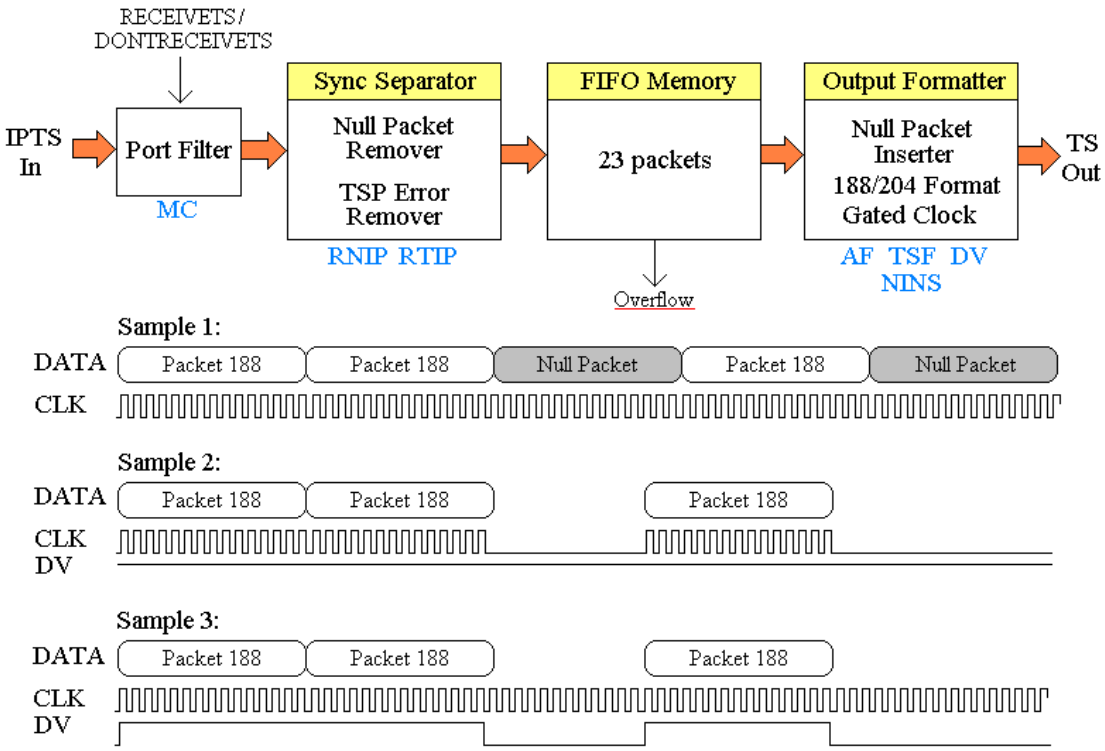



Figure 9. TS Output Channel

Figure 9. shows the block diagram of the TS Output Channel. The function depends on the configuration bits (blue text in figure 9.) in the RECEIVETS instruction. The Port filter selects the correspondent IP stream. The Sync Separator removes null packets and packets with TSP Error flag set to 1 depending on the state of the RNIP and RTIP bits. The IP stream is written into the FIFO Memory, which can store 23 packets at a time. If an overflow event occurs the overflow LED lights up and a trap

message is sent to the host computer (when this function is enabled). Every TS Output Channel has a user programmable Output Formatter. The Output Formatter contains a Null Packet Inserter (to generate continuous stream) a Packet Formatter (188 or 204 bytes) and a Clock Signal Manager (it generates Data Valid signal and gated clock signal). The TS output data rate can be programmed using SETNCO instruction.

The configuration bits of the samples (see the RECEIVETS instruction) are:

| | **NINS** | **AF** | **TSF** | **DV** |
|---|---|---|---|---|
| Sample 1 | 1 | 0 | 0 | - |
| Sample 2 | 0 | 0 | 0 | 0 |
| Sample 3 | 0 | 0 | 0 | 1 |

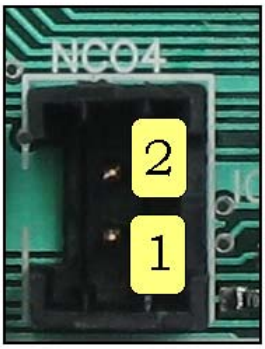
## 4.6. NCOs

The Gigabit Ethernet Controller has 4 independent user programmable Numeric Controlled Oscillators (NCO). Frequency can be set between 120 Hz and 62.5 MHz in 1Hz steps. The NCO frequency is derived from the 125 MHz (50 ppm) system clock. The jitter depends on the division ratio.

NCOs generate clock signals to Transport Stream output channels. Each NCO has an individual connector on the board (M,N,O and P on the block diagram), so all the 4 NCOs can be used in GEC-4I models too. Frequency can be set using SETNCO instruction.

| Pin | Description | Direction |
|---|---|---|
| 1 | GND | |
| 2 | NCO Clock | Output |

NCO Clock impedance: 100 Ω
Max. output current: 10 mA



## 4.7. Parallel Data Interface

The Gigabit Ethernet Controller has a high data rate two-way parallel port (Connector H), through which data can directly be loaded from IP to the device or from the device to IP. Several slave devices can be connected to the bus (figure 10).

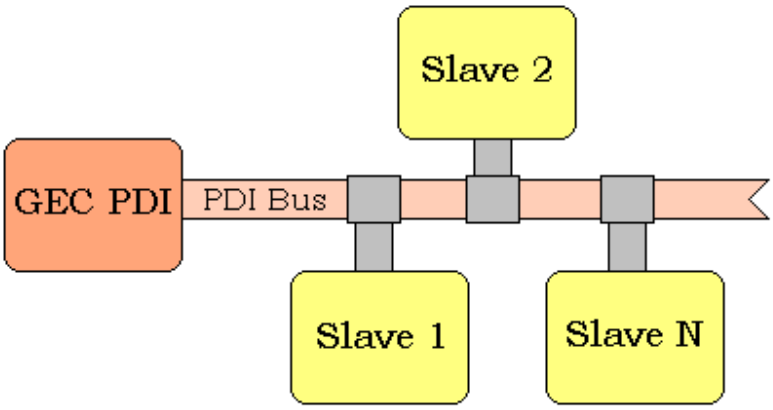
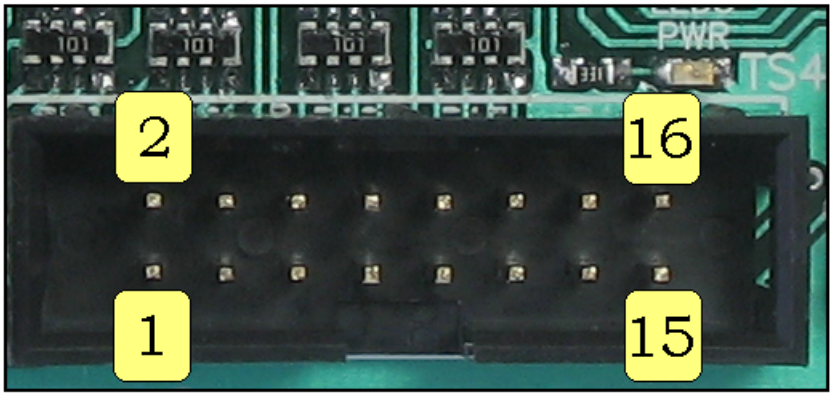



Figure 10. PDI Bus Structure

The Parallel Data Interface (PDI) has an 8-bit bi-directional data bus (DATA 0-7) and control signals: Clock (CLK), Transfer Enable (TE), R/W, IRQ, WAIT and RESET.



| Pin | Description | Direction | Resistors |
|---|---|---|---|
| 1 | GND | | - |
| 2 | DATA 0 | Bi-directional | 2.2 kΩ pullup |
| 3 | DATA 1 | Bi-directional | 2.2 kΩ pullup |
| 4 | DATA 2 | Bi-directional | 2.2 kΩ pullup |
| 5 | DATA 3 | Bi-directional | 2.2 kΩ pullup |
| 6 | VDD (3,3 V) | Output | - |
| 7 | IRQ | Input | 2.2 kΩ pullup |
| 8 | DATA 4 | Bi-directional | 2.2 kΩ pullup |
| 9 | DATA 5 | Bi-directional | 2.2 kΩ pullup |
| 10 | DATA 6 | Bi-directional | 2.2 kΩ pullup |
| 11 | DATA 7 | Bi-directional | 2.2 kΩ pullup |
| 12 | WAIT | Input | 2.2 kΩ pullup |
| 13 | RESET | Output | 2.2 kΩ pulldown |
| 14 | R/W (Read/Write) | Output | - |
| 15 | TE (Transfer Enable) | Output | - |
| 16 | CLK (Clock) | Output | - |

The 8-bit data bus (DATA) is a bi-directional bus, connected to the positive supply voltage (3.3 V) through a pull-up resistor (2.2 kΩ on each line). When the bus is free, lines are HIGH. The output stages of the slave devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

CLK, TE, R/W and RESET signals are outputs generated by the Controller. WAIT and IRQ signals are inputs, connected to the positive supply voltage (3,3 V) through a pull-up resistor (2.2 kΩ).

A Read or a Write operation on the Parallel Data Interface can be performed using PDIREAD or PDIWRITE instructions. Both Read and Write operation start with an address sequence. The controller writes the 8-bit Address and the 32-bit Subaddress to the bus while TE signal is HIGH. Address and Subaddress are used to select the slave device and the memory range. Address sequence is followed by reading or writing the number of data bytes determined in the instruction. Operation is closed by a STOP condition (a LOW to HIGH transition (rising edge) on the CLK line while TE is LOW defines a STOP condition).

The WAIT signal can be asserted by any slave device to delay completion of the current access cycle.

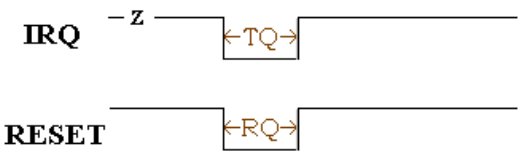



Figure 10. PDI Reset and IRQ

A HIGH to LOW transition on the IRQ signal generates an interrupt in the Controller (figure 10). An IRQ message (see section 6.12.) will be sent to host computer.

| Symbol | Item | Min | Typ | Max |
|---|---|---|---|---|
| TQ | IRQ pulse width | 20 ns | | |
| RQ | RESET pulse width | See RESET instruction | | |

### 4.7.1. Write Operation

During write operation the Controller drives the data lines. The data on the DATA lines must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line will only change when the clock signal on the CLK line is LOW.

The WAIT signal can be asserted by the slave device when CLK is HIGH. The controller samples the WAIT line after the falling edge of the CLK and stops operation until WAIT returns to high or a timeout condition exceeds.

Write sequence is the following (figure 11.):

- Transfer Enable (TE) signal goes to HIGH and remains in HIGH state during the whole write operation. R/W signal remains in LOW state.
- Controller writes Address and Subaddress (address sequence). Slave devices sample the data bus on the rising edge of the clock.
- Controller writes data bytes.
- Transfer Enable (TE) signal returns to LOW. A clock cycle is generated while TE is LOW (STOP condition).

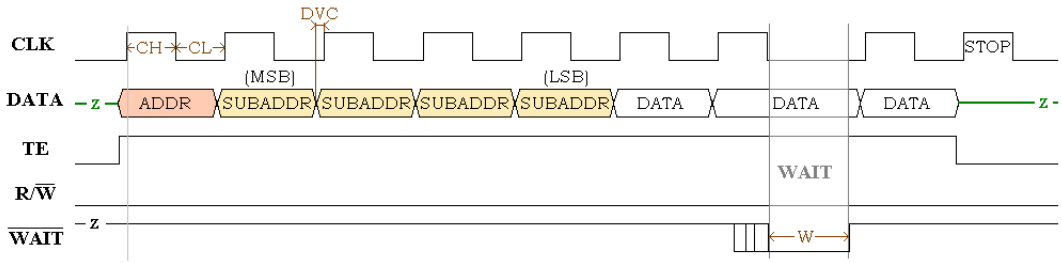



Figure 11. PDI Write

| Symbol | Item (Write) | Min | Typ | Max |
|---|---|---|---|---|
| CH | CLK high time | | 800 ns | |
| CL | CLK low time | 2880 ns[1] | 3680 ns | |
| | *Write data rate* | | | *220 kB/s* |
| DVC | Data Valid before CLK↑ | 40 ns | | |
| W | WAIT pulse width | | | 700 µs |

[1]Before STOP pulse

## 4.7.2. Read Operation

During read operation the Controller drives the data lines only when writing Address and Subaddress. After the address sequence the Controller lets data lines go high impedance state. While reading data bytes slave device must drive the data bus. Controller samples the bus on the falling edge of the CLK. The data on the DATA lines must be stable during the LOW period of the clock.

After the address sequence WAIT signal can be asserted by the slave device when CLK is LOW.

Read sequence is the following (figure 12.):

- Transfer Enable (TE) signal goes to HIGH and remains in HIGH state during the whole read operation. R/W signal goes to HIGH state.
- Controller writes Address and Subaddress (address sequence). Slave devices sample the data bus on the rising edge of the clock.
- Controller generates read clock cycles. Slave device puts data bytes at the rising edge of the clock. Controller samples the bus after every HIGH to LOW transitions on the clock.
- Transfer Enable (TE) and R/W signals return to LOW and a clock cycle is generated. Slave device frees the data bus after the LOW to HIGH transition.
- Controller sends a PDIDATA answer to host computer.

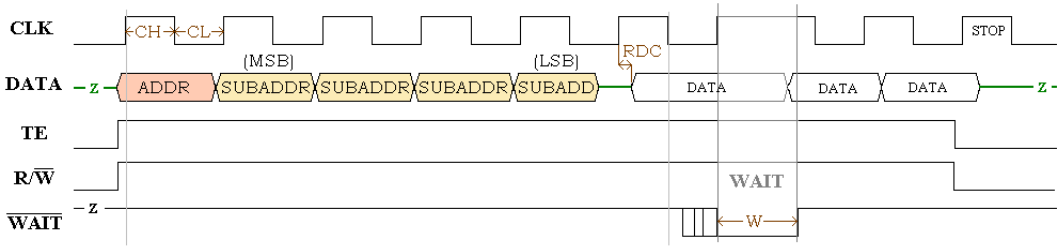



Figure 12. PDI Read

| Symbol | Item (Read) | Min | Typ | Max |
|---|---|---|---|---|
| CH | CLK high time | | 800 ns | |
| CL | CLK low time | 2080 ns[1] | 5280 ns | 10,3 µs[2] |
| | *Read data rate* | | | *160 kB/s* |
| RDC | Data Valid after CLK↑ | 0 ns | | CH |
| W | WAIT pulse width | | | 700 µs |

[1]During Address write
[2]Before the first data byte is read

Notes:

- The level of logical '0' (LOW) is between 0 and 0.45 V.
- The level of logical '1' (HIGH) is between 2.65 and 3.3 V.
- Maximum output current sunk by any data or control pin is 10 mA.

## 4.8. Serial Data Interface

The Gigabit Ethernet Controller has a two-way serial port (Connector J), through which data can directly be loaded from IP to the device or from the device to IP. Several slave devices can be connected to the serial bus. Serial Data Interface (SDI) supports two operating modes:

- CW-Net compatible serial mode
- Normal serial mode

### 4.8.1. CW-Net Compatible Serial Mode

In this mode operation is fully compatible with the CableWorld CW-4900 Ethernet Controller's Serial Data Interface. For details visit www.cableworld.eu. The pinout of the connector in this case is the following:

| Pin | Description (CW-Net compatible serial mode) | Direction | Reseistors |
|---|---|---|---|
| 1 | Serial Read (SR) | Input | 2.2 kΩ pullup |
| 2 | ENABLE 1 | Output | - |
| 3 | ENABLE 2 | Output | - |
| 4 | ENABLE 3 | Output | - |
| 5 | ENABLE 4 | Output | - |
| 6 | ACK | Input | 2.2 kΩ pullup |
| 7 | RESET | Output | - |
| 8 | Serial Write (SW) | Output | - |
| 9 | Clock (CLK) | Output | - |
| 10 | GND | - | - |

To load and read data through the SDI interface use the ENABLEON, ENABLEOFF, LOADDATA, SINGLELOADDATA and READDATA instructions.

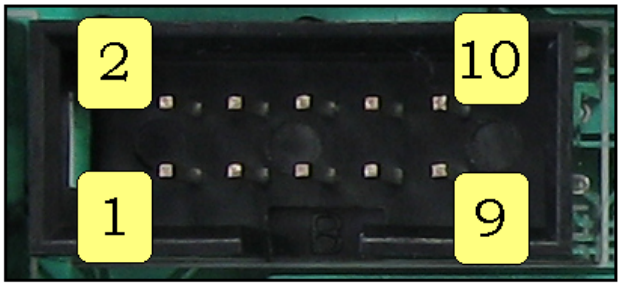
### 4.8.2. Normal Serial Mode

Normal serial mode is very similar to PDI protocol. The differences are:

- There is no WAIT signal implemented.
- Data signal is not bi-directional. Serial Read (SR) is used to read data from slave devices and Serial Write (SW) is used to load data into slave devices. (The output stages of slave devices connected to

the SR wire must have an open-drain or open-collector to perform the wired-AND function.)

- The data bus (SR and SW signals) is serial MSB first.
- Controller sends a SDIDATA answer to host computer after read operation.




| Pin | Description (normal serial mode) | Direction | Resistors |
|---|---|---|---|
| 1 | Serial Read (SR) | Input | 2.2 kΩ pullup |
| 2 | Transfer Enable (TE) | Output | - |
| 3 | R/W | Output | - |
| 4 | (not used) | - | - |
| 5 | (not used) | - | - |
| 6 | IRQ | Input | 2.2 kΩ pullup |
| 7 | RESET | Output | - |
| 8 | Serial Write (SW) | Output | - |
| 9 | Clock (CLK) | Output | - |
| 10 | GND | - | - |

SDI interface can be written or read using WRITESDI and READSDI instructions.

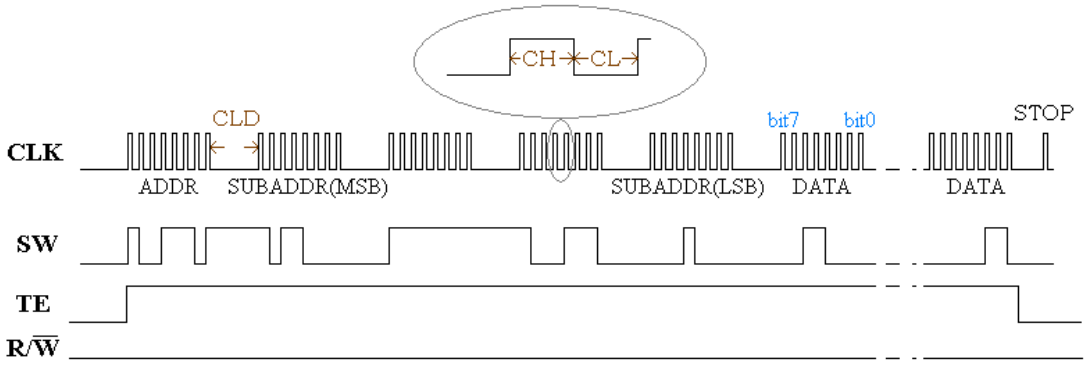



Figure 13. SDI Write

| Symbol | Item (Write) | Min | Typ | Max |
|---|---|---|---|---|
| CH | CLK high time | | 160 ns | |
| CL | CLK low time | | 960 ns | |
| CLD | CLK low between two data bytes | | 6720 ns | |
| | *Write data rate* | | *70 kB/s* | |
| DVC | Data Valid before CLK↑ | 100 ns | | |

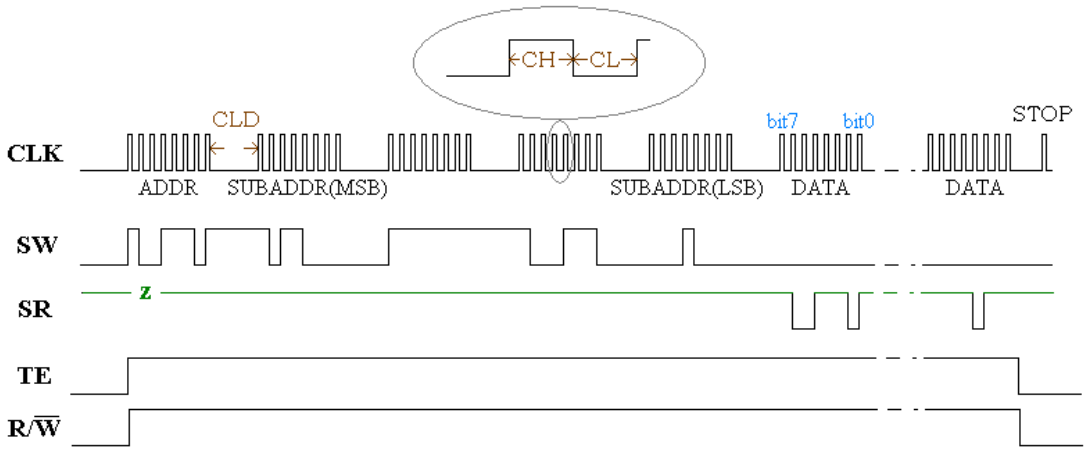



Figure 14. SDI Read

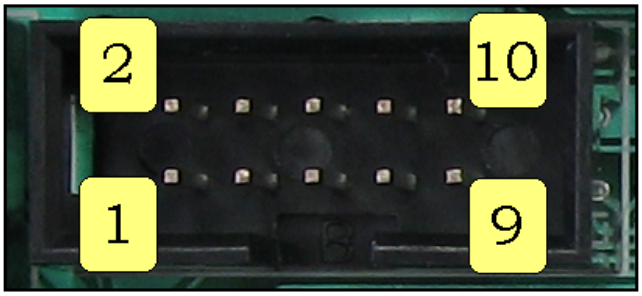
| Symbol | Item (Read) | Min | Typ | Max |
|---|---|---|---|---|
| CH | CLK high time | | 160 ns | |
| CL | CLK low time | | 960 ns | |
| CLD | CLK low between two data bytes | | 8480 ns | |
| | *Write data rate* | | *60 kB/s* | |

Notes:

- The level of logical '0' (LOW) is between 0 and 0.45 V.
- The level of logical '1' (HIGH) is between 2.65 and 3.3 V.
- Maximum output current sunk by any data or control pin is 10 mA.

## 4.9. Selector

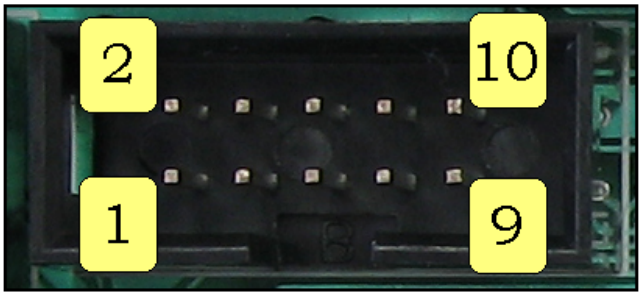
The Selector port (connector I) is a user programmable 9-bit output port. It represents a value between 0 and 511. Output pins (SELECTOR 8..0) can be programmed using SETSELECTOR instruction. The value of the port is stored in the controller's EEPROM (see SAVESELECTOR instruction), so the last value will be loaded during power up. Each pin can be cleared or set individually with CLESRSELECTORBIT and SETSELECTORBIT instructions.




| Pin | Description | Direction |
|---|---|---|
| 1 | SELECTOR 0 | Output |
| 2 | SELECTOR 1 | Output |
| 3 | SELECTOR 2 | Output |
| 4 | SELECTOR 3 | Output |
| 5 | SELECTOR 4 | Output |
| 6 | SELECTOR 5 | Output |
| 7 | SELECTOR 6 | Output |
| 8 | SELECTOR 7 | Output |
| 9 | SELECTOR 8 | Output |
| 10 | GND | - |

## 4.10. General Purpose Output

General Purpose Output (GPO) port (connector K) is a user programmable 8-bit output port. It represents a value between 0 and 255. Output pins (GPO 7..0) can be programmed using SETGPO instruction. The value of the port is stored in the controller's EEPROM (see SAVEGPO instruction), so the last value will be loaded during power up. Each pin can be cleared or set individually with CLEARGPOBIT and SETGPOBIT instructions.

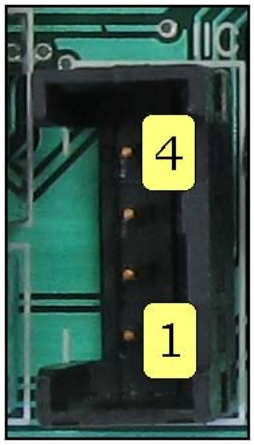



| Pin | Description | Direction |
|---|---|---|
| 1 | GPO 0 | Output |
| 2 | GPO 1 | Output |
| 3 | GPO 2 | Output |
| 4 | GPO 3 | Output |
| 5 | GPO 4 | Output |
| 6 | GPO 5 | Output |
| 7 | GPO 6 | Output |
| 8 | GPO 7 | Output |
| 9 | VDD (3,3 V) | Output |
| 10 | GND | - |

## 4.11. IIC Interface

The Gigabit Ethernet Controller has an IIC (Inter Integrated Circuit – I²C) interface (Connector L), through which data can directly be loaded from IP to an IIC compatible device or from an IIC compatible device to IP. The IIC-bus has two wires, serial data (SDA) and serial clock (SCL). Each device connected to the bus is recognized by a unique address and can operate as either a transmitter or receiver, depending on the function of the device. The controller is the master on the bus (slave mode isn't supported). It implements the master functions of the 7-bit addressing mode. The master initiates a data transfer on the bus and generates all of the serial clock pulses and the Start and Stop conditions. At that time, any device addressed is considered a slave. For details about IIC interface and operation see the Philips IIC-bus specification version 2.1.

| Pin | Description | Direction | Resistors |
|---|---|---|---|
| 1 | GND | - | - |
| 2 | SDA | Bi-directional | 2.2 kΩ pullup |
| 3 | SCL | Output | 2.2 kΩ pullup |
| 4 | VDD (3.3 V) | Output | - |




IIC interface supports single read and write sequences using READIIC and WRITEIIC instructions (figure 15.). In case of read user can set whether the controller generates acknowledge after the last data byte or not (ACK bit).

Detailed ACK answer contains an IIC Error byte (byte 365). IIC Error is cleared automatically before every IIC data transfer. Bit 0 (ADA) is set if acknowledge isn't received after address byte. Bit 1 (WRA) is set if acknowledge isn't received after every data bytes (in case of write).


Figure 15. IIC Error Byte

IIC clock frequency can be set for 100 kHz, 400 kHz or 1 MHz IIC operation using SETIICCLOCK instruction.

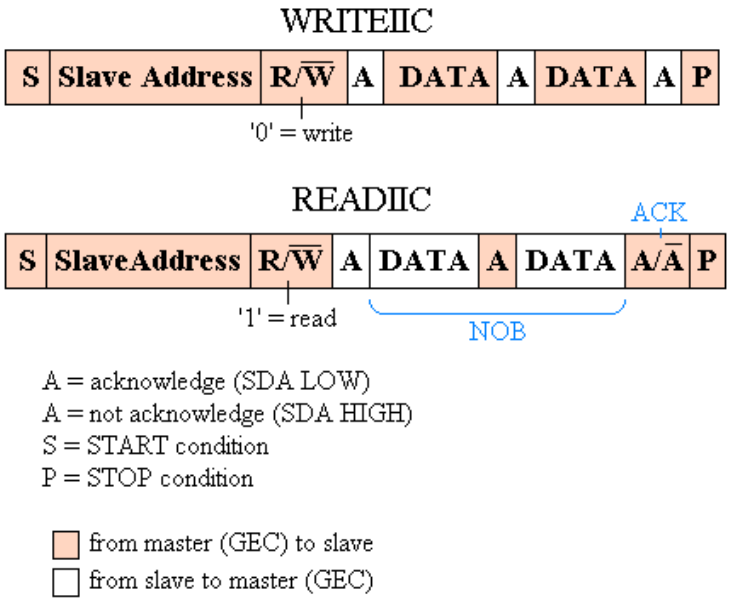
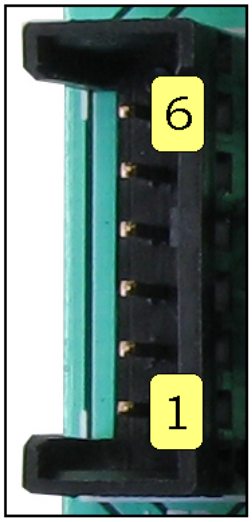



Figure 16. IIC Write and Read Sequences

## 4.12. Status LEDs

Status LEDs port (connector Q) can be used to directly drive LEDs on the front panel of the equipment (serial resistors required).

| Pin | Description | Direction |
|---|---|---|
| 1 | GND | - |
| 2 | GIGABIT | Output |
| 3 | OVERFLOW | Output |
| 4 | POWERON | Output |
| 5 | ACT | Output |
| 6 | LINK | Output |



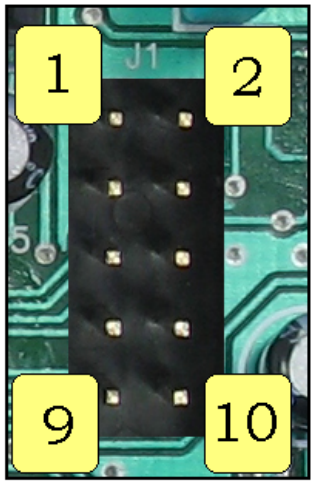

GIGABIT port is high at 1000Base-T connection. OVERFLOW is high (for 0.5 second) if an overflow event occurs either on an input TS channel or an output TS channel. POWERON is high after power up. ACT and LINK ports refer to the LAN connector's LEDs.

## 4.13. Overflow LEDs

The Overflow LEDs port (connector R) is an optional 10-pin jumper on the board used to signal overflow events on the particular TS channels.

| Pin | Description | Direction |
|---|---|---|
| 1 | TS Input Channel 1 overflow | Output |
| 2 | TS Input Channel 2 overflow | Output |
| 3 | GND | - |
| 4 | *Not connected* | - |
| 5 | TS Input Channel 3 overflow | Output |
| 6 | TS Input Channel 4 overflow | Output |
| 7 | TS Output Channel 1 overflow | Output |
| 8 | TS Output Channel 2 overflow | Output |
| 9 | TS Output Channel 3 overflow | Output |
| 10 | TS Output Channel 4 overflow | Output |

An overflow event causes a high pulse of half-second width on the respective pin. Ports can be directly connected to LEDs (serial resistors required).



## 4.14. Trap Function

The Trap function is under development!

## 4.15. Reset Defaults Jumper

User could reset default settings by shorting Reset Defaults jumper (connector T). It is useful when device is locked and user forgot the key, or the device's IP address is unknown. To reset default settings follow these steps:

- Switch off (to power off state) the device.
- Short the Reset Defaults jumper.
- Switch on the device and wait for 5 seconds (or more). The power on LED is blinking.
- Switch off the device again.
- Open the jumper.

Settings changed:

- IP: 10.123.13.101
- MAC: CW-Auto mode
- Network mask: 255.0.0.0
- TS port interval: 57000 – 59999
- Configuration word: 0x0003

# 5. Instruction Set

General instructions:

| | |
|---|---|
| NOP | Opcode = 0x00 |
| RESET | Opcode = 0x01 |
| WAIT | Opcode = 0x02 |
| SENDACK | Opcode = 0x03 |
| LASTINSTRUCTION | Opcode = 0x04 |
| LOCK | Opcode = 0x05 |
| UNLOCK | Opcode = 0x06 |

Configuration instructions:

| | |
|---|---|
| SETSERIAL | Opcode = 0x10 |
| SETTYPE | Opcode = 0x11 |
| SETUSERTEXT | Opcode = 0x12 |
| SETCONFIG | Opcode = 0x13 |

Network instructions:

| | |
|---|---|
| SETGATEWAY | Opcode = 0x20 |
| SETNETMASK | Opcode = 0x21 |
| SETPMAC | Opcode = 0x22 |
| SETSMAC | Opcode = 0x23 |
| SETIP | Opcode = 0x24 |
| SETARPADVERTISE | Opcode = 0x25 |
| SETTRAP | Opcode = 0x26 |

Transport Stream Input instructions:

| | |
|---|---|
| SENDTS | Opcode = 0x30 |
| DONTSENDTS | Opcode = 0x31 |

Transport Stream Output instructions:

| | |
|---|---|
| SETNCO | Opcode = 0x40 |
| DONTRECEIVETS | Opcode = 0x41 |
| RECEIVETS | Opcode = 0x42 |
| SETTSPORTINTERVAL | Opcode = 0x43 |
| SETIGMPREPORTTIME | Opcode = 0x44 |

Selector instructions:

| | |
|---|---|
| SETSELECTOR | Opcode = 0x50 |
| SETSELECTORBIT | Opcode = 0x51 |
| CLEARSELECTORBIT | Opcode = 0x52 |
| SAVESELECTOR | Opcode = 0x53 |

GPO instructions:

| | |
|---|---|
| SETGPO | Opcode = 0x60 |
| SETGPOBIT | Opcode = 0x61 |
| CLEARGPOBIT | Opcode = 0x62 |
| SAVEGPO | Opcode = 0x63 |

Parallel Data Interface instructions:

| | |
|---|---|
| WRITEPDI | Opcode = 0x70 |
| READPDI | Opcode = 0x71 |

Serial Data Interface instructions:

| | |
|---|---|
| WRITESDI | Opcode = 0x80 |
| READSDI | Opcode = 0x81 |
| ENABLEON | Opcode = 0x82 |
| ENABLEOFF | Opcode = 0x83 |
| LOADDATA | Opcode = 0x84 |
| SINGLELOADDATA | Opcode = 0x85 |
| READDATA | Opcode = 0x86 |

IIC instructions:

| | |
|---|---|
| SETIICCLOCK | Opcode = 0x90 |
| WRITEIIC | Opcode = 0x91 |
| READIIC | Opcode = 0x92 |

HTTP instructions (future release):

| | |
|---|---|
| LOADHTTPROM | Opcode = 0xA0 |

Gigabit Ethernet Controller answers:

| | |
|---|---|
| ACK | Opcode = 0xF0 |
| IRQ | Opcode = 0xF1 |
| PDIDATA | Opcode = 0xF2 |
| SDIDATA | Opcode = 0xF3 |
| IICDATA | Opcode = 0xF4 |
| TRAP | Opcode = 0xF5 |

## 5.1. General Instructions

NOP instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x00 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x00 | | | | | |

Description:

Do nothing.

RESET instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x01 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x02 | | | | | |
| 4 | ResetType | | 0x00 – Parallel Data Interface Reset<br>0x01 – System Reset<br>0x02 – Serial Data Interface Reset | | | | | |
| 5 | ResetTime | | | | | | | |

Description:

The System Reset resets the whole controller. Reset time is 400 ms.

The ResetTime determines the width of the reset impulse during any Interface Reset:

$$t_{\text{Reset Width}} = \text{ResetTime [ms]}$$

WAIT instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x02 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x02 | | | | | |
| 4 | WaitX | | | | | | | |
| 5 | WaitY | | | | | | | |

Description:

Wait before processing the next instruction.

$t_{Wait\ Time}$ = (WaitX * 100) + WaitY [ms]

SENDACK instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x03 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x01 | | | | | |
| 4 | ACKType | | 0x00 – Single ACK<br>0x01 – Detailed ACK | | | | | |

Description:

Send an ACK message to the host computer (see section 5.12).

LASTINSTRUCTION instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x04 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x00 | | | | | |

Description:

This is the last instruction is the chain. This instruction can be followed by any user data byte in the UDP packet.

LOCK instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x05 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x08 | | | | | |
| 4-11 | LockKey (MSB..LSB) | | | | | | | |

Description:

The LOCK instruction locks the device with the LockKey. The locked device performs SENDACK and UNLOCK instructions only. Don't forget the LockKey! Without it you can not unlock the device via UDP. If you forget the LockKey use the Reset Defaults Jumper to unlock the device (section 4.14).

UNLOCK instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x06 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x08 | | | | | |
| 4-11 | LockKey (MSB..LSB) | | | | | | | |

Description:

Use the UNLOCK instruction to unlock a locked device. You must use the same LockKey, which was used to lock the device.

## 5.2. Configuration Instructions

SETSERIAL instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x10 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x04 | | | | | |
| 4 | SerialNumber (MSB) | | | | | | | |
| 5 | SerialNumber | | | | | | | |
| 6 | SerialNumber | | | | | | | |
| 7 | SerialNumber (LSB) | | | | | | | |

Description:

Set and store the Serial Number. SerialNumber is a 4-byte unsigned integer. (Note: with CW-Net instructions you can set/read the lower 2 bytes only).

SETTYPE instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x11 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x02 | | | | | |
| 4 | Type (MSB) | | | | | | | |
| 5 | Type (LSB) | | | | | | | |

Description:

Set and store the Type. Type is a 2-byte unsigned integer.

SETUSERTEXT instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **1** | Opcode | | 0x12 | | | | | |
| **2** | Length (High) | | 0x00 | | | | | |
| **3** | Length (Low) | | 0x0F | | | | | |
| **4-18** | UserText (15 characters) | | | | | | | |

Description:

Set and store the UserText. UserText is a user-defined string in the DDToIP header (in device answers).

SETCONFIGURATION instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **1** | Opcode | | 0x13 | | | | | |
| **2** | Length (High) | | 0x00 | | | | | |
| **3** | Length (Low) | | 0x01 | | | | | |
| **4** | | | | | | | CW2 | CW1 |

Description:

Set and store the lower byte of the 2-byte Configuration word. The upper byte is read only (see ACK answer).

The Gigabit Ethernet Controller is CW-Net compatible. If both CW1 and CW2 bits are set it performs all the CW-Net instructions.

CW1: Processing CW-Net ‘replace’ instructions.

CW2: Processing all other CW-Net instructions.

## 5.3. Network Instructions

SETGATEWAY instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x20 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x11 | | | | | |
| 4 | 0 | 0 | 0 | 0 | GWMODE | | | |
| 5-20 | GatewayIP (MSB..LSB) | | | | | | | |

Description:

Set and store the gateway parameters.

GWMODE: 0 – There is no gateway in the network
1 – Normal (GatewayIP must be set)
2 – Auto (future release)
3..15 – Reserved

The GatewayIP is the IP address of the gateway. (Note: in case of IPv4 addresses only the lower 4 bytes are used.)

SETNETMASK instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x21 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x10 | | | | | |
| 4-19 | NetworkMask (MSB..LSB) | | | | | | | |

Description:

Set and store the network mask. If a packet's destination address is outside the local subnet, the Gigabit Ethernet Controller sends the packet to the destination through the default gateway. (Note: in case of IPv4 addresses only the lower 4 bytes are used. E.g.: 0.0.0.0.0.0.0.0.0.0.0.0.255.255.255.0)

SETPMAC instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x22 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x07 | | | | | |
| 4 | MACMode | | 0 – CW Auto<br>1 – Manual | | | | | |
| 5-10 | MAC (MSB..LSB) | | | | | | | |

Description:

Set and store the primary MAC address and mode. For details see section 4.3.1.

SETSMAC instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x23 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x07 | | | | | |
| 4 | 0x00 | | | | | | | |
| 5-10 | MAC (MSB..LSB) | | | | | | | |

Description:

Set and store the secondary MAC address.

SETIP instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x24 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x10 | | | | | |
| 4-19 | IP (MSB..LSB) | | | | | | | |

Description:

Set and store the controller's IP address. (Note: in case of IPv4 address only the lower 4 bytes are used.)

SETARPADVERTISE instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x25 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x01 | | | | | |
| 4 | AdvertiseTime | | | | | | | |

Description:

Set and store the ARP Advertising function parameters. If the ARP Advertising function is on, the device periodically sends broadcast ARP reply messages ("the device is at its IP address").

If AdvertiseTime is set to zero (0x00) this function is switched off. Otherwise:

$$T_{ARP\ period} = \text{AdvertiseTime [s]}$$

SETTRAP instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x26 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x15 | | | | | |
| 4 | TON | SNMP | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | TI4 | TI3 | TI2 | TI1 | TO4 | TO3 | TO2 | TO1 |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TX1 |
| 7-22 | IP | | | | | | | |
| 23 | Port | | | | | | | |

Description:

Set and store the Trap function. Trap messages are generated automatically when an unmasked trap source (TX,TO or TI) occurs.

TON: 1/0 – Trap function is on/off

SNMP: 1 – Trap message format is SNMP (Port is 162)
0 – Trap message format is UDP (Port must be set)

TXn: 1/0 – Enable/disable external Trap source (future release)

TOn: 1/0 – Enable/disable Trap on Output Channel n overflow

TIn: 1/0 – Enable/disable Trap on Input Channel n overflow

IP: The Trap message's destination IP

Port: The Trap message's destination port in case of UDP format

## 5.4. Transport Stream Input Instructions

SENDTS instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode 0x30 | | | | | | | |
| 2 | Length (MSB) 0x00 | | | | | | | |
| 3 | Length (LSB) 0x1D | | | | | | | |
| 4 | Channel 1..4 | | | | | | | |
| 5 | 0 | 0 | 0 | 0 | 0 | ALWY | FRMT | DV |
| 6 | CWNetSize (MSB) / IPTVMode(MSB) | | | | | | | |
| 7 | CWNetSize (LSB) / IPTVMode(LSB) | | | | | | | |
| 8 | IPF | 0 | 0 | 0 | DESTMODE | | | |
| 9-14 | MAC (MSB..LSB) | | | | | | | |
| 15-30 | IP (MSB..LSB) | | | | | | | |
| 31-32 | Port (MSB..LSB) | | | | | | | |

Description:

Send the Transport Stream (for details see section 4.3.).

ALWY: 1 – Always send the TS. The controller automatically starts sending TS after system reset or power on condition.
0 – Send the TS.

FRMT: 1 – IPTV Format (byte 6 and 7 are IPTVMode)
0 – CW-Net Format (byte 6 and 7 are CWNetSize)

DV: 1/0 – Enable/disable Data Valid pin

IPTVMode is a 2-byte unsigned integer (when FRMT = 1). The lower byte (LSB) is 0x00. The higher byte determines the IPTV packet parameters:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NUMOFPACKET | | | 0 | 0 | RTSP | RNP | TSF |

NUMOFPACKET: Number of TS packets in a UDP packet (between 1 and 7).

RTSP: 1 – Remove TS packets with TSP Error Flag = 1

RNP: 1 – Remove null packets

TSF: 1 – TS packet format is 204 byte
0 – TS packet format is 188 byte

CWNetSize is a 2-byte unsigned integer (when FRMT = 0). It is the data size of the CW-Net packet in bytes (128..1440, default is 1428).

IPF: 1 – Use IPv6 protocol (future release)
0 – Use IPv4 protocol

DESTMODE: Selects the UDP packet's destination (0..4).

0 – Send TS to Me
1 – Send TS to Broadcast
2 – Send TS to IP
3 – Send TS to Multicast
4 – Send TS to Manual address

MAC: Destination MAC Address (6 bytes) in case of Multicast or Manual mode (DESTMODE = 3 or 4).

IP: Destination IP Address (16 bytes) in case of IP, Multicast or Manual mode (DESTMODE = 2, 3 or 4). (Note: in case of IPv4 addresses only the lower 4 bytes are used.)

Port: Destination UDP Port (2 bytes). Always must be set.

DONTSENDTS instruction

| **Byte** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **1** | Opcode | | 0x31 | | | | | |
| **2** | Length (MSB) | | 0x00 | | | | | |
| **3** | Length (LSB) | | 0x01 | | | | | |
| **4** | Channel | | 1..4 | | | | | |

Description:

Stop sending the Transport Stream.

## 5.5. Transport Stream Output Instructions

SETNCO instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x40 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x05 | | | | | |
| 4 | Channel | | 1..4 | | | | | |
| 5 | Frequency (MSB) | | | | | | | |
| 6 | Frequency | | | | | | | |
| 7 | Frequency | | | | | | | |
| 8 | Frequency (LSB) | | | | | | | |

Description:

Set and store the NCO frequency. Frequency is a 4-byte unsigned integer in Hz. (Note: this will be the clock frequency of the corresponding Transport Stream output.)

$Frequency_{min}$ = 120 Hz

$Frequency_{max}$ = 62500000 Hz = 62.5 MHz

DONTRECEIVETS instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x41 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x01 | | | | | |
| 4 | Channel | | 1..4 | | | | | |

Description:

Disable the selected Transport Stream Output channel. All output pins are forced to LOW.

RECEIVETS instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x42 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x14 | | | | | |
| 4 | Channel | | 1..4 | | | | | |
| 5 | 0 | MC | AF | TSF | DV | NINS | RTIP | RNIP |
| 6-7 | Port (MSB..LSB) | | | | | | | |
| 8-23 | MulticastIP (MSB..LSB) | | | | | | | |

Description:

Set and store the selected Transport Stream Output channel parameters.

MC: 1 – Receive multicast TS
0 – Receive non-multicast TS

AF: 1 – Auto Format (use IP Stream format 188/204)
0 – Manual format (TSF)

TSF: 1 – TS packet format is 204 byte (if AF = 0)
0 – TS packet format is 188 byte (if AF = 0)

DV: 1 – Data Valid pin enabled (continuous TS clock)
0 – Gated TS clock

NINS: 1/0 – Null packet inserter on/off

RTIP: 1 – Remove TS packets with TSP Error Flag = 1 from the IP stream

RNIP: 1 – Remove null packets from the IP stream

SETTSPORTINTERVAL instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x43 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x04 | | | | | |
| 4-5 | PortLow (MSB..LSB) | | | | | | | |
| 6-7 | PortHi (MSB..LSB) | | | | | | | |

Description:

Set and store the TS Port Interval. The factory default value for TS Port Interval is: 57000-59999. For details see section 4.3.1.

SETIGMPREPORTTIME instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **1** | Opcode | | 0x44 | | | | | |
| **2** | Length (MSB) | | 0x00 | | | | | |
| **3** | Length (LSB) | | 0x01 | | | | | |
| **4** | IGMPReportTime | | | | | | | |

Description:

Set and store the IGMP report time. If the IGMPReportTime is set to zero (0x00) this function is switched off. Otherwise:

$T_{IGMP\ report\ period}$ = IGMPReportTime * 400 [ms]

## 5.6. Selector Instructions

SETSELECTOR instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x50 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | SELECTOR (MSB) | | | | | | | |
| 5 | SELECTOR (LSB) | | | | | | | |
| 6 | SAVE | 0 | 0 | 0 | MATH | | | |

Description:

Set the Selector state depending on the MATH value.

MATH: 0 – Selector port will be SELECTOR

1 – Logical AND between SELECTOR and the actual value of the port

2 – Logical OR between SELECTOR and the actual value of the port

3 – Logical XOR between SELECTOR and the actual value of the port

SAVE: 1 – Save the new Selector state to EEPROM

SETSELECTORBIT instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x51 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | 0x00 | | | | | | | |
| 5 | BIT | | 0..8 | | | | | |
| 6 | 0x00 | | | | | | | |

Description:

Set the selected Selector bit.

CLEARSELECTORBIT instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x52 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | 0x00 | | | | | | | |
| 5 | BIT | | 0..7 | | | | | |
| 6 | 0x00 | | | | | | | |

Description:

Clear the selected Selector bit.

SAVESELECTOR instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x53 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x00 | | | | | |

Description:

Save the state of the Selector port.

## 5.7. GPO Instructions

SETGPO instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x60 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | 0x00 | | | | | | | |
| 5 | GPO | | | | | | | |
| 6 | SAVE | 0 | 0 | 0 | MATH | | | |

Description:

Set the GPO state depending on the MATH value.

MATH: 0 – GPO port will be SELECTOR

1 – Logical AND between GPO and the actual value of the port

2 – Logical OR between GPO and the actual value of the port

3 – Logical XOR between GPO and the actual value of the port

SAVE: 1 – Save the new GPO state to EEPROM

SETGPOBIT instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x61 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | 0x00 | | | | | | | |
| 5 | BIT | | 0..7 | | | | | |
| 6 | 0x00 | | | | | | | |

Description:

Set the selected GPO bit.

CLEARGPOBIT instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x62 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | 0x00 | | | | | | | |
| 5 | BIT | | 0..7 | | | | | |
| 6 | 0x00 | | | | | | | |

Description:

Clear the selected GPO bit.

SAVEGPO instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x63 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x00 | | | | | |

Description:

Save the state of the GPO port.

## 5.8. Parallel Data Interface Instructions

WRITEPDI instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x70 | | | | | |
| 2 | Length (MSB) | | | | | | | |
| 3 | Length (LSB) | | | | | | | |
| 4 | ADDR | | | | | | | |
| 5-8 | SUBADDR (MSB..LSB) | | | | | | | |
| 9-n | DATA | | | | | | | |

Description:

Write the data bytes (DATA) to the selected Address (ADDR) and Subaddress (SUBADDR) through the Parallel Data Interface.

READPDI instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x71 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x07 | | | | | |
| 4 | ADDR | | | | | | | |
| 5-8 | SUBADDR (MSB..LSB) | | | | | | | |
| 9-10 | NOB | | 1..1447 | | | | | |

Description:

Read NOB (number of data bytes) data bytes from the selected Address (ADDR) and Subaddress (SUBADDR) through the Parallel Data Interface. Data read from the slave device is sent to the host computer encapsulated in a PDIDATA answer message.

## 5.9. Serial Data Interface Instructions

WRITESDI instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **1** | Opcode | | 0x80 | | | | | |
| **2** | Length (MSB) | | | | | | | |
| **3** | Length (LSB) | | | | | | | |
| **4** | ADDR | | | | | | | |
| **5-8** | SUBADDR (MSB..LSB) | | | | | | | |
| **9-n** | DATA | | | | | | | |

Description:

Write the data bytes (DATA) to the selected Address (ADDR) and Subaddress (SUBADDR) through the Serial Data Interface (using Normal serial mode).

READSDI instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **1** | Opcode | | 0x81 | | | | | |
| **2** | Length (MSB) | | 0x00 | | | | | |
| **3** | Length (LSB) | | 0x07 | | | | | |
| **4** | ADDR | | | | | | | |
| **5-8** | SUBADDR (MSB..LSB) | | | | | | | |
| **9-10** | NOB | | 1..1447 | | | | | |

Description:

Read NOB (number of data bytes) data bytes from the selected Address (ADDR) and Subaddress (SUBADDR) through the Serial Data Interface (using Normal serial mode). Data read from the slave device is sent to the host computer encapsulated in an SDIDATA answer message.

ENABLEON instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x82 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x01 | | | | | |
| 4 | ADDR | | 1..15 | | | | | |

Description:

This instruction is the same as the *Enable On* CW-Net instruction. For details visit www.cableworld.eu.

ENABLEOFF instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x83 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x00 | | | | | |

Description:

This instruction is the same as the *Enable Off* CW-Net instruction. For details visit www.cableworld.eu.

LOADDATA instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x84 | | | | | |
| 2 | Length (MSB) | | | | | | | |
| 3 | Length (LSB) | | | | | | | |
| 4-n | DATA | | | | | | | |

Description:

This instruction is the same as the *LoadData* CW-Net instruction. For details visit www.cableworld.eu.

SINGLELOADDATA instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x85 | | | | | |
| 2 | Length (MSB) | | | | | | | |
| 3 | Length (LSB) | | | | | | | |
| 4 | ADDR | | 1..15 | | | | | |
| 5-n | DATA | | | | | | | |

Description:

This instruction is the same as the *Single LoadData* CW-Net instruction. For details visit www.cableworld.eu.

READDATA instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x86 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | ADDR | | 1..15 | | | | | |
| 5-6 | NOB | | | | | | | |

Description:

This instruction is the same as the *ReadData* CW-Net instruction. For details visit www.cableworld.eu.

## 5.10. IIC Instructions

SETIICCLOCK instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x90 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x01 | | | | | |
| 4 | FRQDIV | | | | | | | |

Description:

Set and store the IIC bus clock speed.

$$F_{IIC\ Clock} = \frac{6250000}{FRQDIV + 1}\ [\text{Hz}]$$

$F_{max}$ = 6.25 MHz
$F_{min}$ = 24.5 kHz

WRITEIIC instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x91 | | | | | |
| 2 | Length (MSB) | | | | | | | |
| 3 | Length (LSB) | | | | | | | |
| 4 | SLAVEADDR | | | | | | | X |
| 5-n | DATA | | | | | | | |

Description:

Write the data bytes (DATA) to the selected slave address (SLAVEADDR) through the IIC Interface.

READIIC instruction

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode | | 0x92 | | | | | |
| 2 | Length (MSB) | | 0x00 | | | | | |
| 3 | Length (LSB) | | 0x03 | | | | | |
| 4 | SLAVEADDR | | | | | | | ACK |
| 5-6 | NOB | | | | | | | |

Description:

Read NOB (number of data bytes) data bytes from the selected slave address (SLAVEADDR) through the IIC Interface. Data read from the slave device is sent to the host computer encapsulated in an IICDATA answer message.

ACK: 1 - Last data byte acknowledged
0 - Last data byte not acknowledged

## 5.12. Gigabit Ethernet Controller Answers

ACK answer

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Opcode 0xF0 | | | | | | | |
| 2 | Length (MSB) | | | | | | | |
| 3 | Length (LSB)<br>For Single ACK length is 16 (0x0010).<br>For Detailed ACK length is 509 (0x01FD) or 1021 (0x3FD). | | | | | | | |
| 4 | Version High (VH) | | | | | | | |
| 5 | Version Low (VL)<br>VH and VL determine the controller's version number in VH.VL format. VL can be between 0 and 99 (in decimal format). If VH = 2 and VL = 0 version is 2.00. If VH = 2 and VL = 10 version is 2.10. | | | | | | | |
| 6-9 | Serial Number (MSB..LSB) | | | | | | | |
| 10-11 | Type (MSB..LSB) | | | | | | | |
| 12-13 | Configuration (MSB..LSB)<br>bit 15..9: Reserved<br>bit 8: Device locked (1)<br>bit 7..2: Reserved<br>bit 1: CW-Net compatibility (all other instructions)<br>bit 0: CW-Net compatibility (replace instructions) | | | | | | | |
| 14-15 | Selector (MSB..LSB) | | | | | | | |
| 16 | GPO | | | | | | | |
| 17 | External Trap State | | | | | | | |
| 18 | Overflow bit 7..4: overflow in TS Input Channel 4..1<br>bit 3..0: overflow in TS Output Channel 4..1 | | | | | | | |
| 19 | Link<br>1 – 10 Mpbs<br>2 – 100 Mpbs<br>3 – 1000 Mpbs | | 0 | 0 | 0 | Model<br>0 – 4I<br>1 – 4O<br>2 – 2D<br>3 – 2L<br>4..7 - Reserved | | |
| 20 | MAC Mode 0 – CW Auto<br>1 – Manual | | | | | | | |
| 21-26 | Primary MAC (MSB..LSB) | | | | | | | |
| 27-42 | Primary IP (MSB..LSB) | | | | | | | |
| 43 | Reserved (0x00) | | | | | | | |
| 44-49 | Secondary MAC (MSB..LSB) | | | | | | | |
| 50-67 | Reserved (0x00) | | | | | | | |

| | |
|---|---|
| **68** | Gateway Mode 0 – There is no Gateway in the network<br>1 – Manual mode |
| **69** | Gateway State 0 – There is no Gateway in the network<br>1 – Gateway known<br>2 – Searching Gateway MAC<br>3 – Searching Gateway IP |
| **70-75** | Gateway MAC (MSB..LSB)<br>Valid if Gateway State = 1. |
| **76-91** | Gateway IP (MSB..LSB) |
| **92-107** | Network Mask (MSB..LSB) |
| **108** | ARP Timer |
| **109** | Reserved (0x00) |
| **110-115** | TS Input Channel 1 Destination MAC (MSB..LSB) |
| **116-131** | TS Input Channel 1 Destination IP (MSB..LSB) |
| **132-133** | TS Input Channel 1 Destination Port (MSB..LSB) |
| **134** | TS Input Channel 1 Destination Mode |
| **135** | TS Input Channel 1 State<br>0 – Stopped<br>1 – Sending TS<br>2 – Searching destination MAC<br>3 – Gateway unknown and destination outside the local network (waiting) |
| **136-138** | TS Input Channel 1 Mode (byte 2..0)<br>byte 2 – Same as the 5th byte in the SENDTS instruction<br>byte 1..0 – CWNetSize/IPTVMode |
| **139-141** | Reserved (0x00) |
| **142-147** | TS Input Channel 2 Destination MAC |
| **148-163** | TS Input Channel 2 Destination IP (MSB..LSB) |
| **164-165** | TS Input Channel 2 Destination Port (MSB..LSB) |
| **166** | TS Input Channel 2 Destination Mode |
| **167** | TS Input Channel 2 State |
| **168-170** | TS Input Channel 2 Mode |
| **171-173** | Reserved (0x00) |
| **174-179** | TS Input Channel 3 Destination MAC |
| **180-195** | TS Input Channel 3 Destination IP (MSB..LSB) |
| **196-197** | TS Input Channel 3 Destination Port (MSB..LSB) |
| **198** | TS Input Channel 3 Destination Mode |
| **199** | TS Input Channel 3 State |
| **200-202** | TS Input Channel 3 Mode |
| **203-205** | Reserved (0x00) |
| **206-211** | TS Input Channel 4 Destination MAC |

| | |
|---|---|
| **212-227** | TS Input Channel 4 Destination IP (MSB..LSB) |
| **228-229** | TS Input Channel 4 Destination Port (MSB..LSB) |
| **230** | TS Input Channel 4 Destination Mode |
| **231** | TS Input Channel 4 State |
| **232-234** | TS Input Channel 4 Mode |
| **235-237** | Reserved (0x00) |
| **238-239** | TS Port High (MSB..LSB) |
| **240-241** | TS Port Low (MSB..LSB) |
| **242** | IGMP Report Time |
| **243** | IsIGMPSwitch 1 – IGMP switch found |
| **244-249** | IGMP Switch MAC (MSB..LSB), if IsIGMPSwitch = 1 |
| **250-265** | IGMP Switch IP (MSB..LSB) , if IsIGMPSwitch = 1 |
| **266-281** | TS Output Channel 1 Multicast IP (MSB..LSB) |
| **282-283** | TS Output Channel 1 Port (MSB..LSB) |
| **284** | TS Output Channel 1 Mode<br>Same as the 5th byte in the RECEIVETS instruction. |
| **285-289** | Reserved (0x00) |
| **290-305** | TS Output Channel 2 Multicast IP (MSB..LSB) |
| **306-307** | TS Output Channel 2 Port (MSB..LSB) |
| **308** | TS Output Channel 2 Mode |
| **309-313** | Reserved (0x00) |
| **314-329** | TS Output Channel 3 Multicast IP (MSB..LSB) |
| **330-331** | TS Output Channel 3 Port (MSB..LSB) |
| **332** | TS Output Channel 3 Mode |
| **333-337** | Reserved (0x00) |
| **338-353** | TS Output Channel 4 Multicast IP (MSB..LSB) |
| **354-355** | TS Output Channel 4 Port (MSB..LSB) |
| **356** | TS Output Channel 4 Mode |
| **357-363** | Reserved (0x00) |
| **364** | IIC FrqDiv |
| **365** | IIC Error |
| **366-367** | Reserved (0x00) |
| **368-371** | NCO1 Frequency (MSB..LSB) |
| **372-375** | NCO2 Frequency (MSB..LSB) |
| **376-379** | NCO3 Frequency (MSB..LSB) |
| **380-383** | NCO4 Frequency (MSB..LSB) |
| **384-385** | Instruction Packet Counter (MSB..LSB)<br>The counter is automatically incremented after an instruction packet (DDToIP or CW-Net) is processed. |
| **386-391** | Trap MAC (MSB..LSB) |
| **392-407** | Trap IP (MSB..LSB) |

| | |
|---|---|
| **408-409** | Trap Port (MSB..LSB) |
| **410** | Trap Mode |
| **411** | Trap State |
| **412** | External Trap Mask (TX8..TX1) |
| **413** | Overflow Trap Mask (TI4..TI1, TO4..TO1) |
| **414** | External Trap (TX8..TX1) |
| **415** | Overflow Trap (TI4..TI1, TO4..TO1)<br>If a Trap event occurred the corresponding bit is set. |
| **416-512** | Reserved (0x00) |

IRQ answer

| **Byte** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **0** | Opcode | | 0xF1 | | | | | |
| **1** | Length (MSB) | | 0x00 | | | | | |
| **2** | Length (LSB) | | 0x01 | | | | | |
| **3** | IRQ Source | | 0 – PDI<br>1 – SDI | | | | | |

PDIDATA answer

| **Byte** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **0** | Opcode | | 0xF2 | | | | | |
| **1** | Length (MSB) | | | | | | | |
| **2** | Length (LSB) | | | | | | | |
| **3-n** | Data | | | | | | | |

SDIDATA answer

| **Byte** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **0** | Opcode | | 0xF3 | | | | | |
| **1** | Length (MSB) | | | | | | | |
| **2** | Length (LSB) | | | | | | | |
| **3-n** | Data | | | | | | | |

IICDATA answer

| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | Opcode | | 0xF4 | | | | | |
| 1 | Length (MSB) | | | | | | | |
| 2 | Length (LSB) | | | | | | | |
| 3-n | Data | | | | | | | |
| m | | | | | | | | AER |

Description:

AER: No ACK impulse received after the address byte.

TRAP answer

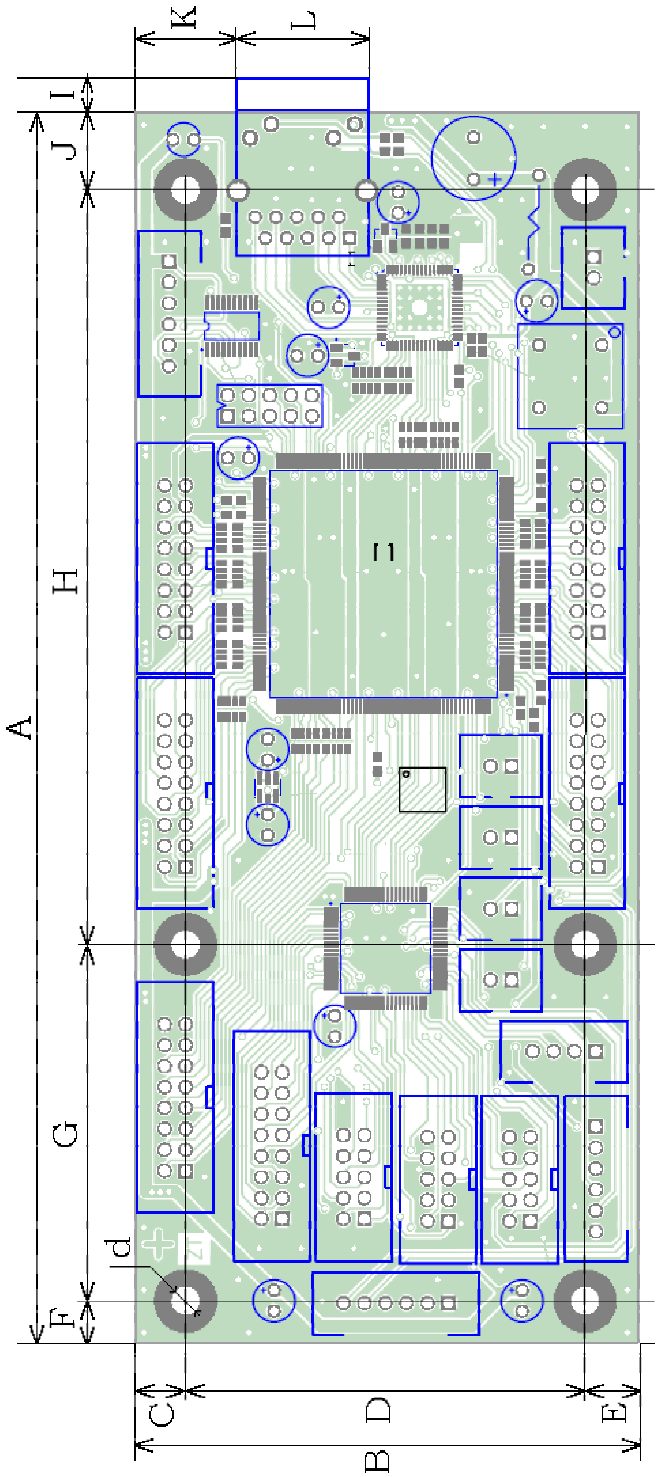
| Byte | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | Opcode | | 0xF5 | | | | | |
| 1 | Length (MSB) | | | | | | | |
| 2 | Length (LSB) | | | | | | | |
| 3-n | The TRAP answer's body is the same as the Detailed ACK answer. | | | | | | | |

# 6. Electrical Characteristics

Recommended operating conditions:

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| VCC (power supply) | 3.18 | 3.3 | 3.43 | V |
| Input current | | | 600 | mA |
| Operating temperature | 0 | | +70 | °C |
| | | | | |

# 7. Mechanical Dimensions




Units: mil [mm]

Tolerance: ±10 %

| | |
|---|---|
| A | 5880 [150] |
| B | 2400 [61] |
| C | 245 |
| D | 1900 [48] |
| E | 255 |
| F | 205 |
| G | 1700 [43] |
| H | 3600 [91] |
| I | 160 [4] |
| J | 375 |
| K | 500 |
| L | 630 |
| d | 126 [3.2] |

Max. height: 800

# 8. Version Information

| Version | Date | Modifications |
|---|---|---|
| 2.00 | 18.03.2007 | Version start.<br>Test version for development. |
| 2.01 | | First official version of the controller. |
| | | |

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